LIGA and its Application to Electrical Interconnects

Rosenberger

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IEEE SW Test Workshop
Semiconductor Wafer Test Workshop
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Outline

Brief introduction to Rosenberger (very brief)

Tutorial of the “UV LIGA Process”

Examples of parts produced with the “UV LIGA Process”

Electrical Interconnects produced with the “UV LIGA Process”

Challenges, Solutions, & Discoveries

What’s next

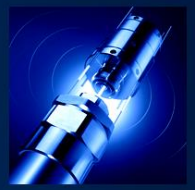
http://en.wikipedia.org/wiki/LIGA

Rosenberger is a Global Engineering & Manufacturing Company

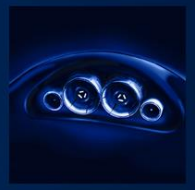
We are industry leaders in high frequency signal delivery

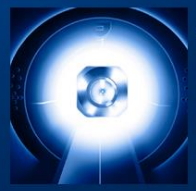
Business Areas — Rosenberger


•Communication
RF-Coaxial Connectors

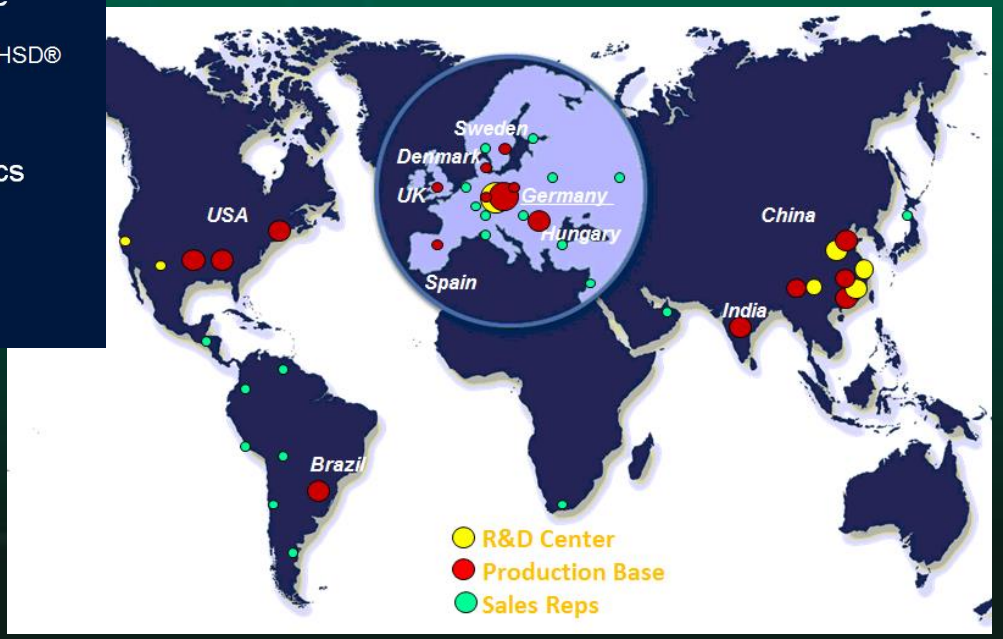

•Communication
SLink Site Solutions


•Test & Measurement


•Automotive
FAKRA
RosenbergerHSD®


•Medical Solutions

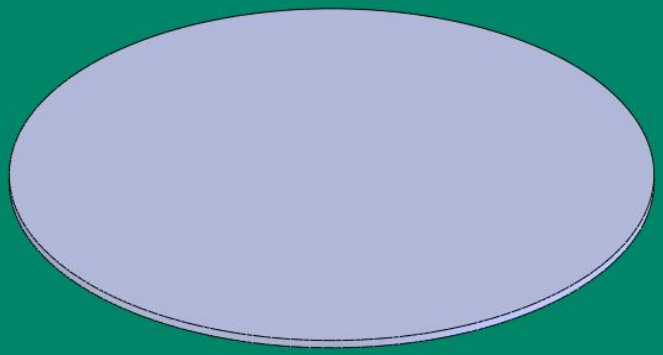

•Fiber Optics



12 Countries
18 Production facilities WW
~4900 Employees WW
Most process lines vertically integrated
Well known and respected as a leader in innovation in all served market segments

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



LIGA the process

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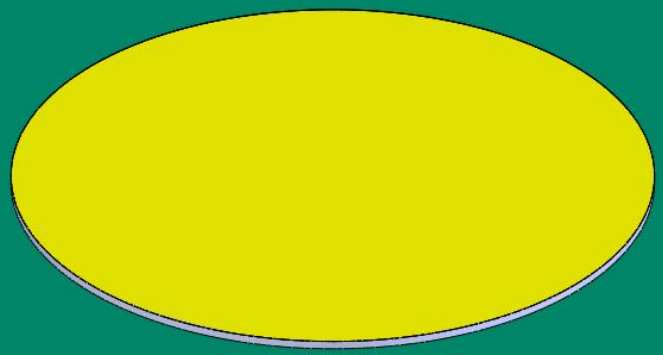
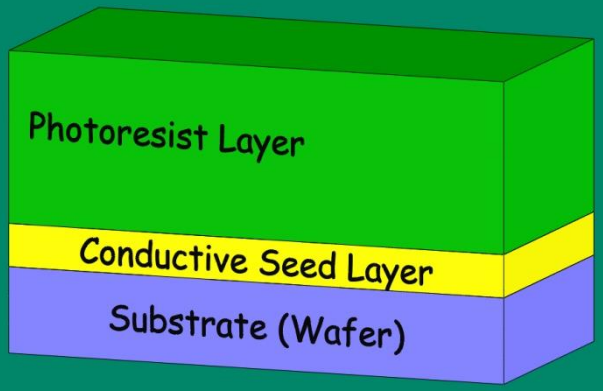
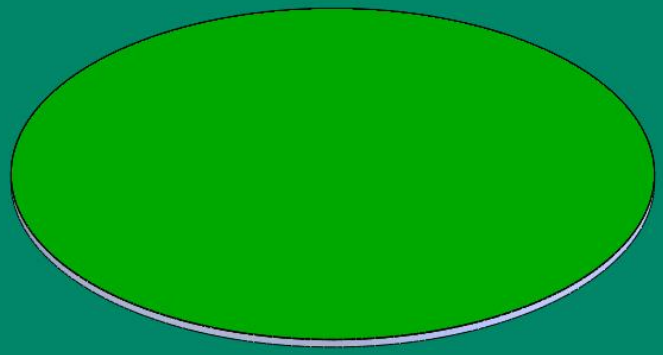


Conductive Seed Layer
Applied with PVD Process

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



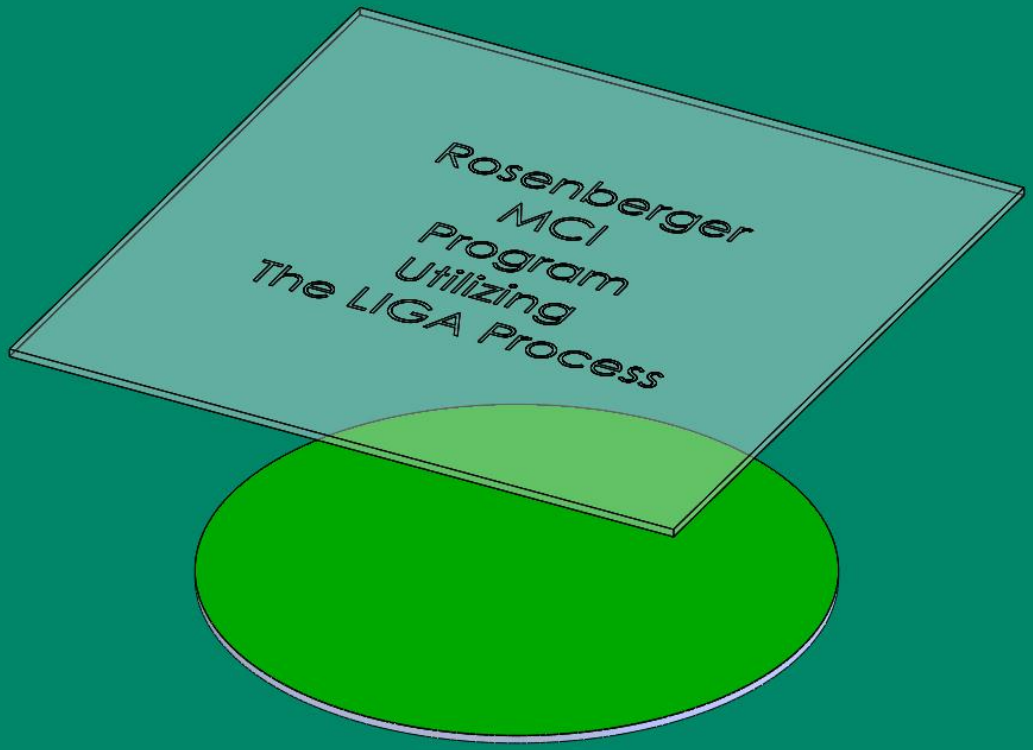


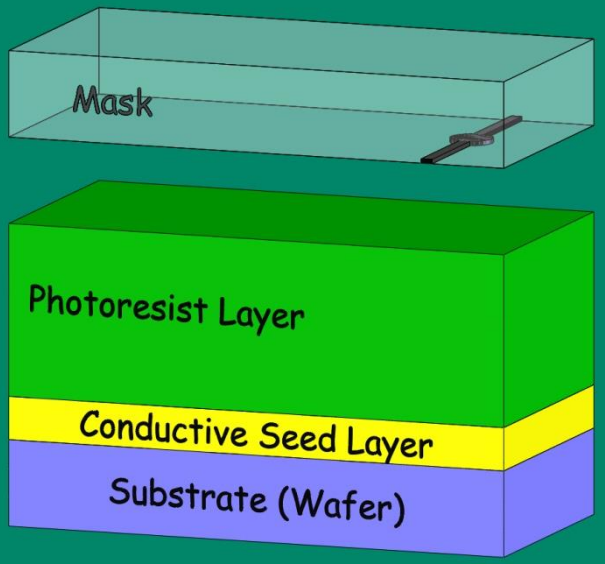
Photoresist applied with
Spin Coat Process

Wafer ready for processing

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

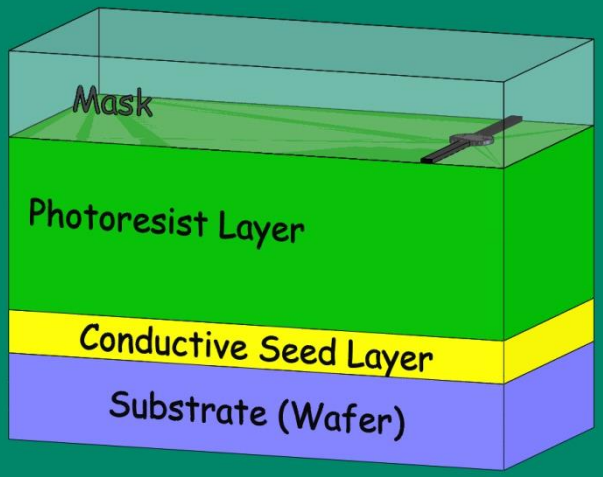




Design and Procure Mask

LIGA the process

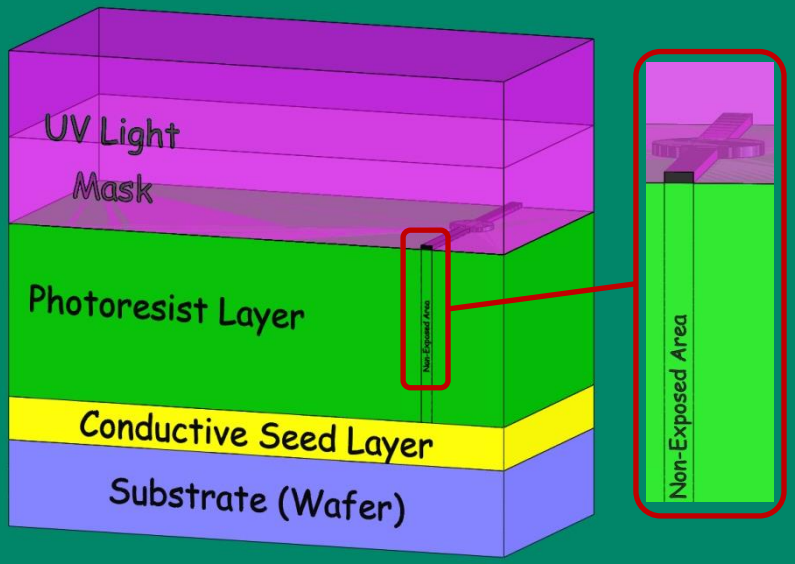
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



Mask is Aligned to Wafer

LIGA the process

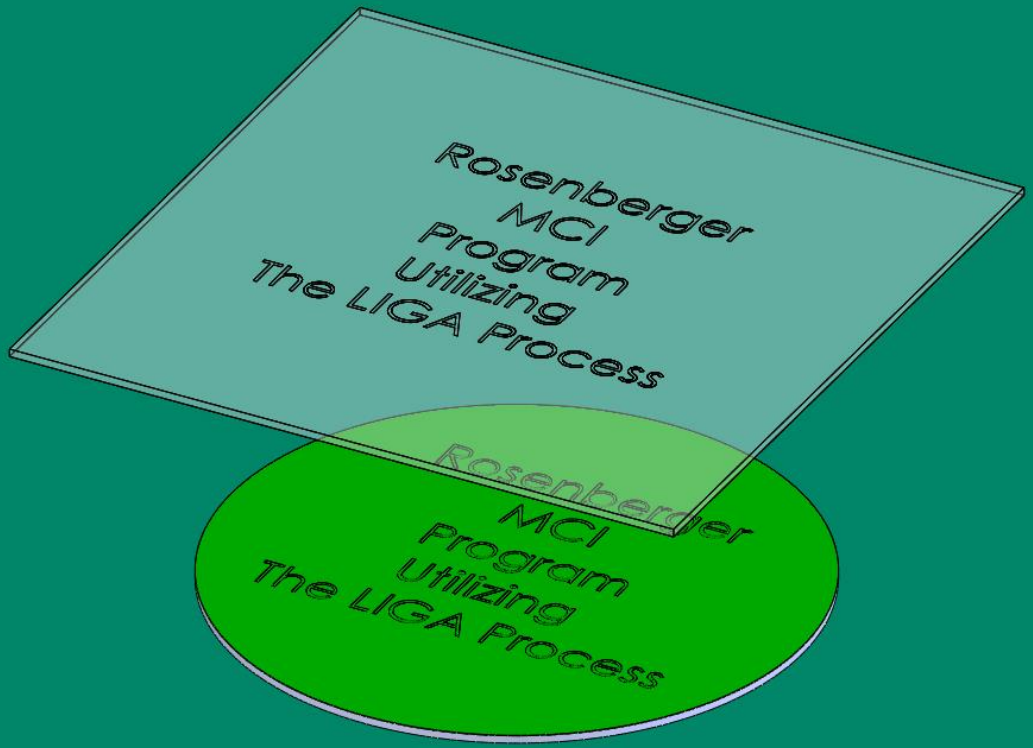
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

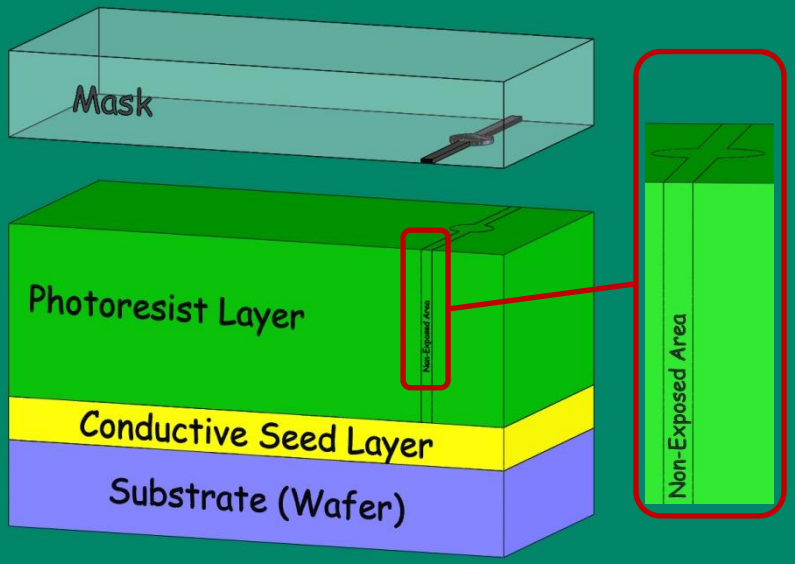


Exposed to a UV Light Source

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

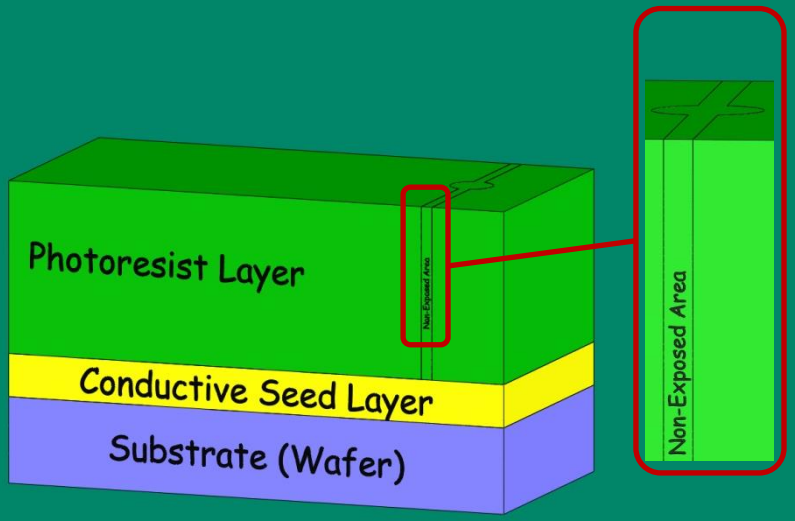




Mask Pattern is Transferred

LIGA the process

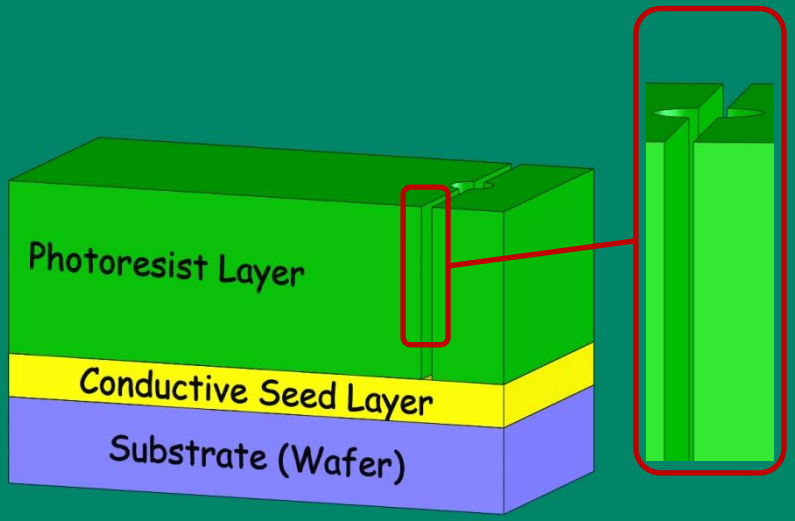
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



Photoresist Is cured
In Curing Process

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

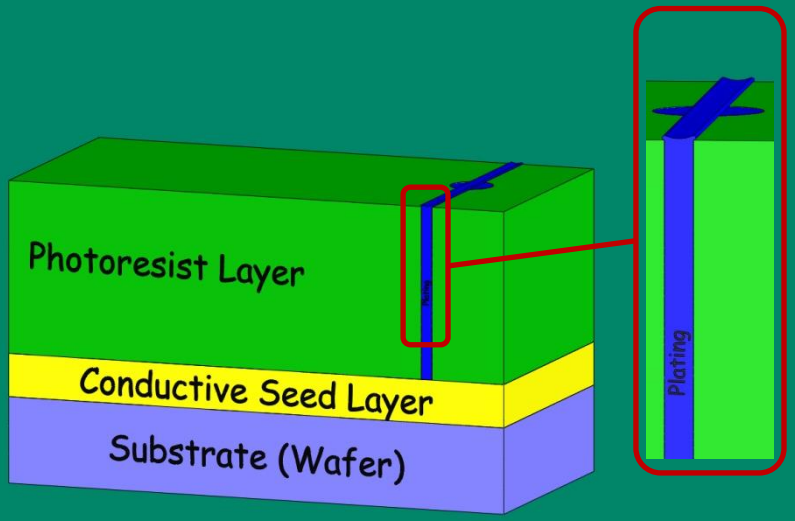


Non-Exposed Photoresist Chemically Remove
(Conductive layer now exposed)

Wafer can now be defined as a Mold

LIGA the process

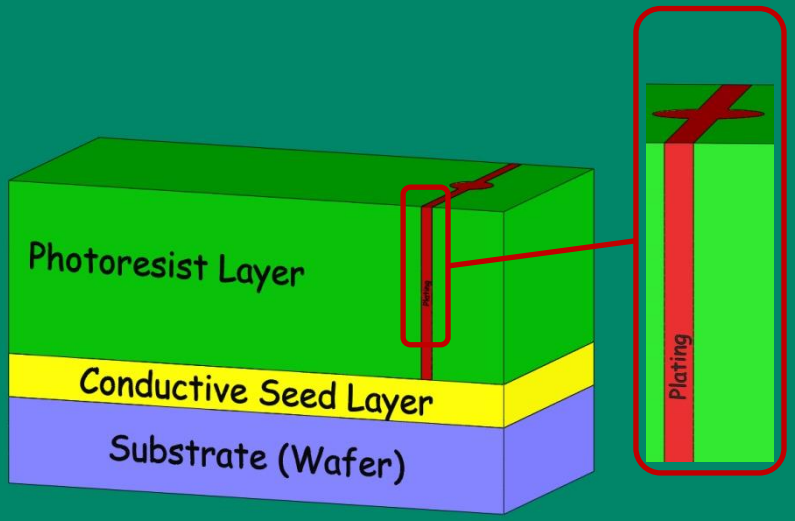
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



Wafer is Plated

LIGA the process

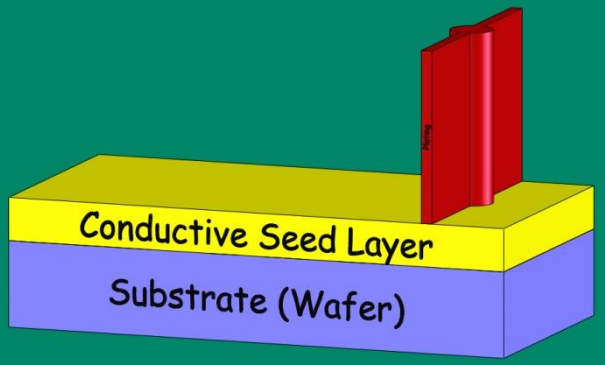
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



Wafer is Lapped to final thickness

LIGA the process

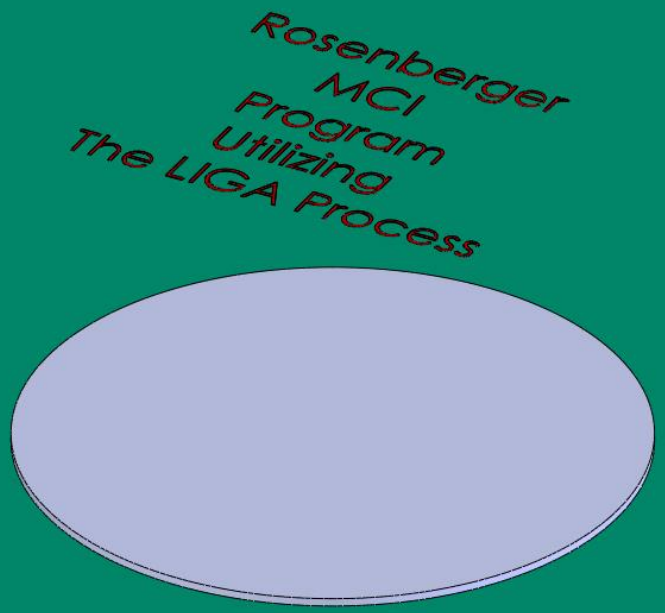
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

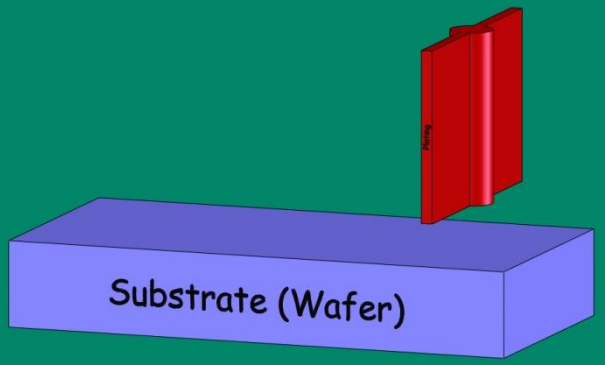


Photoresist Removed with Plasma Etch Process

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

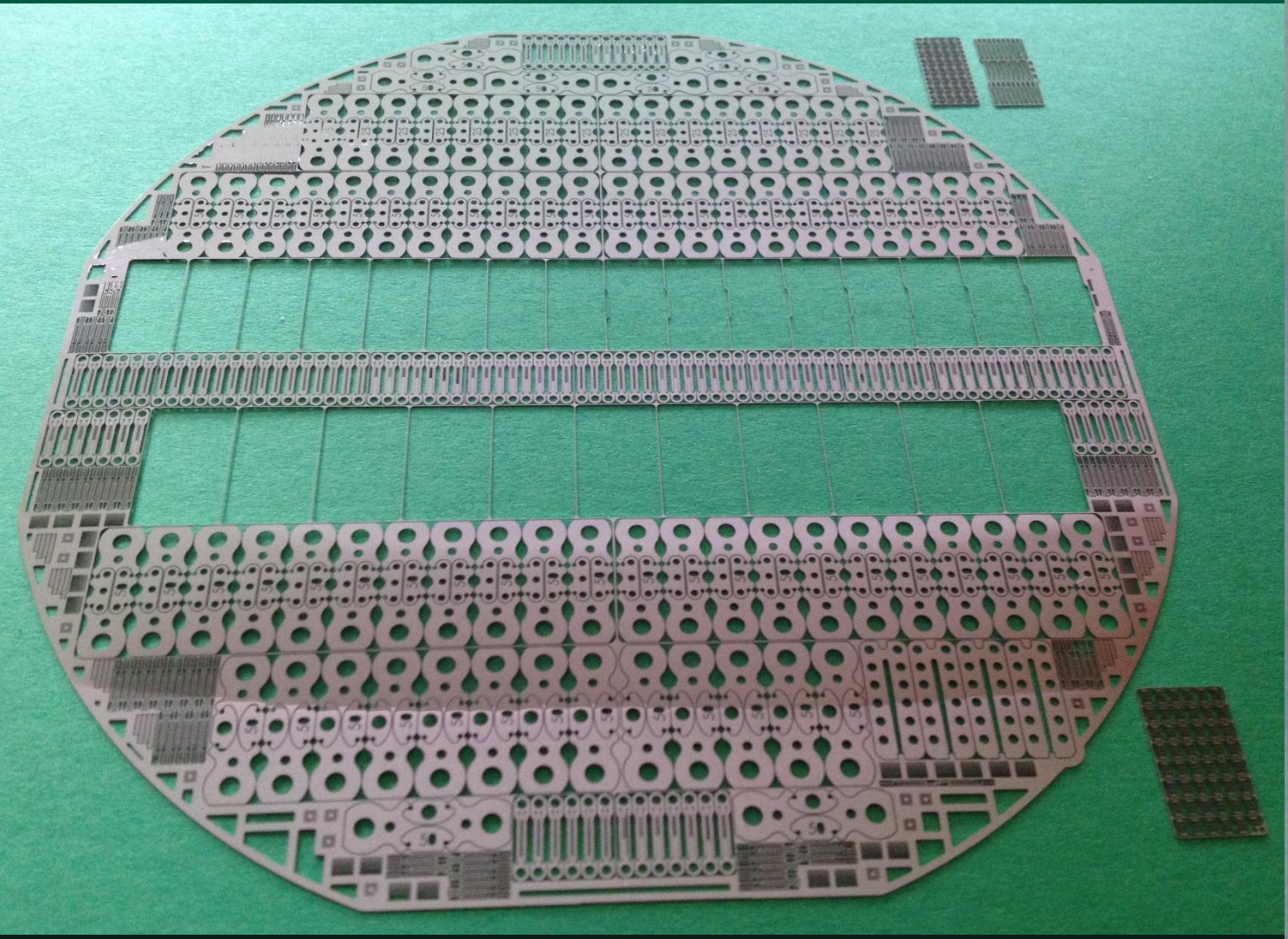


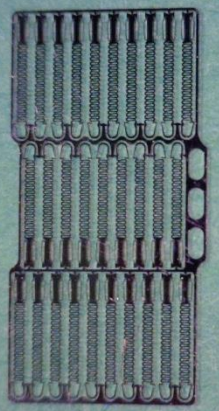


Conductive Seed Layer
Chemically Removed

Parts are released

Example of released wafer





MCI Materials

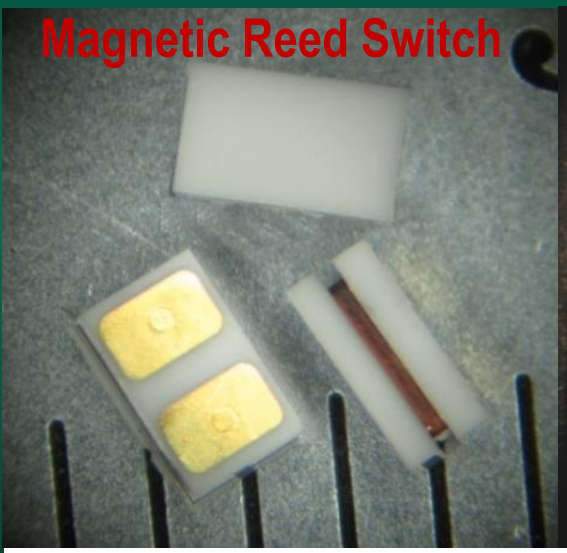
Electroform materials

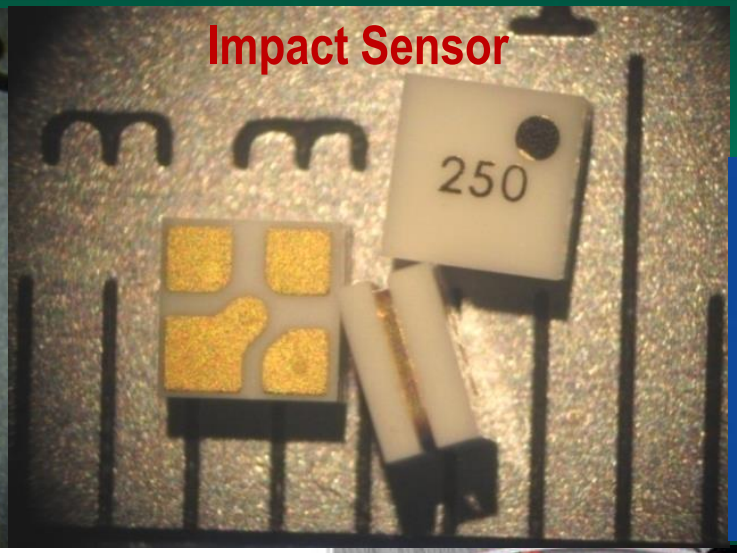
Ni
NiCo
NiP
NiFe
NiW
Au
AuNi
AuCo
Cu
Ag
Others…

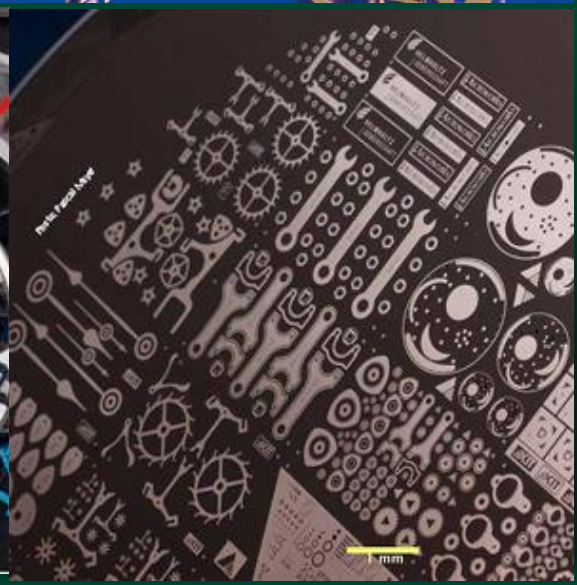
Electroplate only materials
(<5µm)

Ru
Rh
Pd
W
And all of the Electroform list

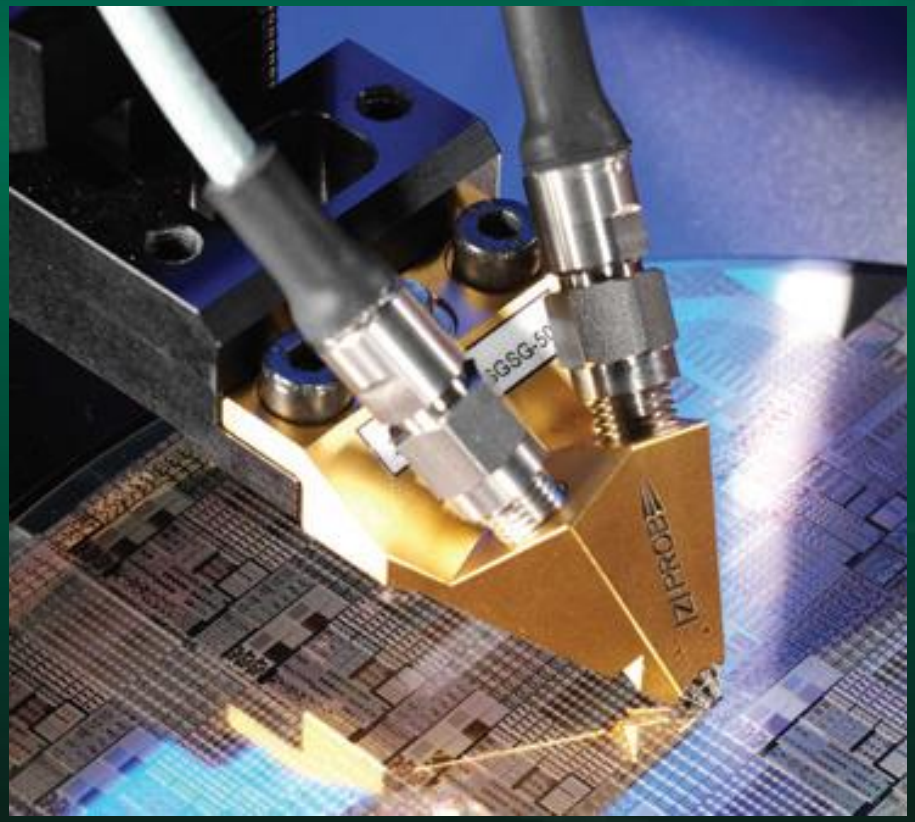
Commercialized LIGA Products







Current Rosenberger LIGA Based Products



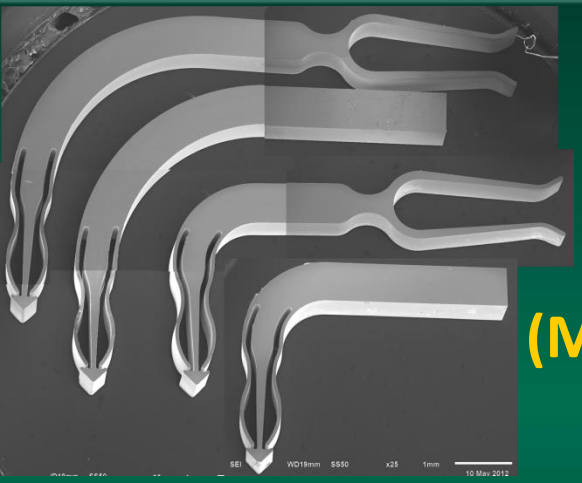
Cascade Microtech Z-Probe

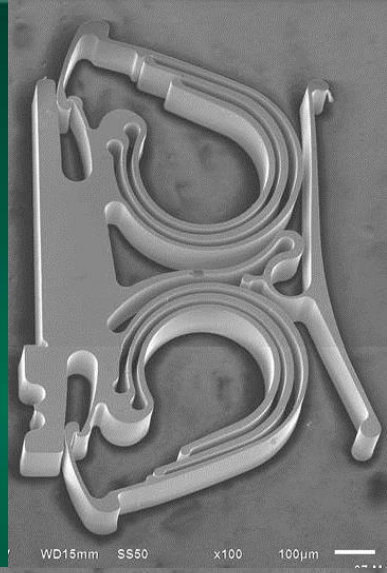
Exclusively developed for Suss MicroTec, now owned by Cascade Microtech Inc.
(2000)

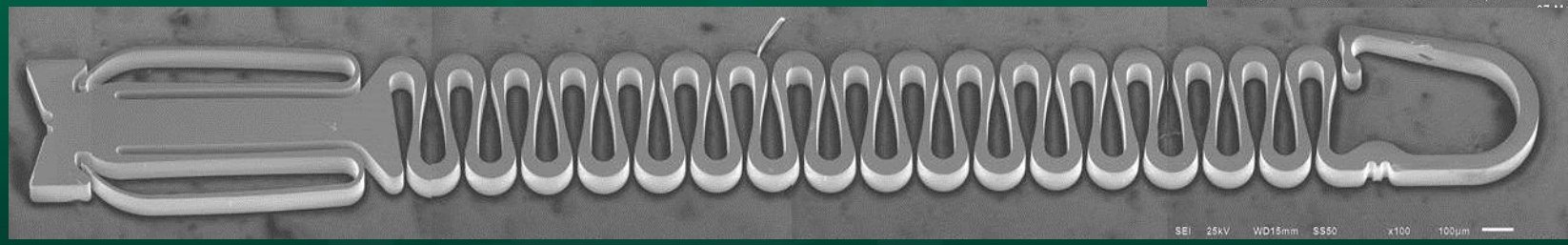
Rosenberger

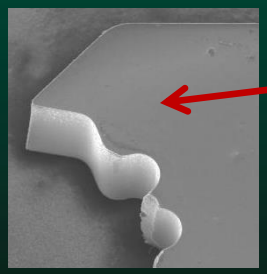
MCI product line

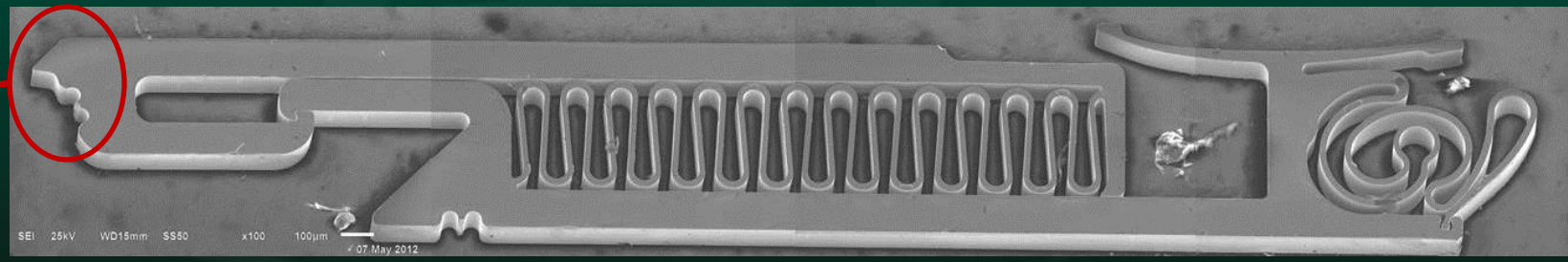
(Monolithic Compliant Interconnects)

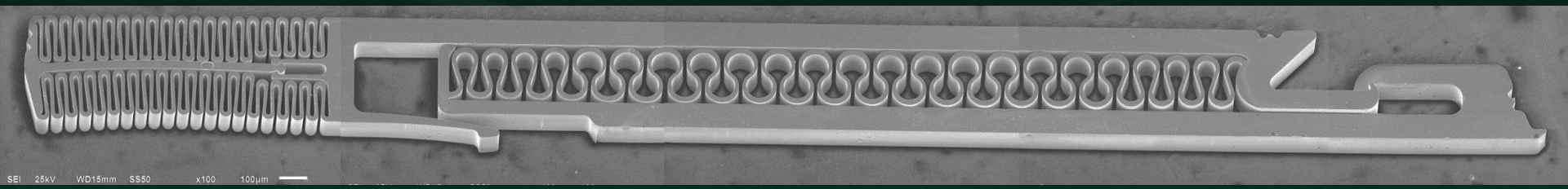












0.8mm Pitch Interposer Array

0.076mm Preload Per Side

0.15mm Usable Travel Per Side

0.30mm Total Usable Travel

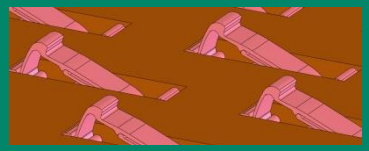
0.150mm Thickness

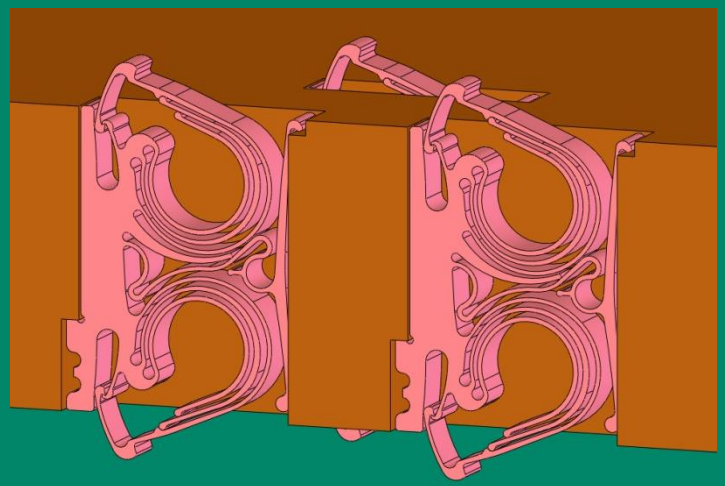
0.065mm Contact to DUT Scrub Per Side

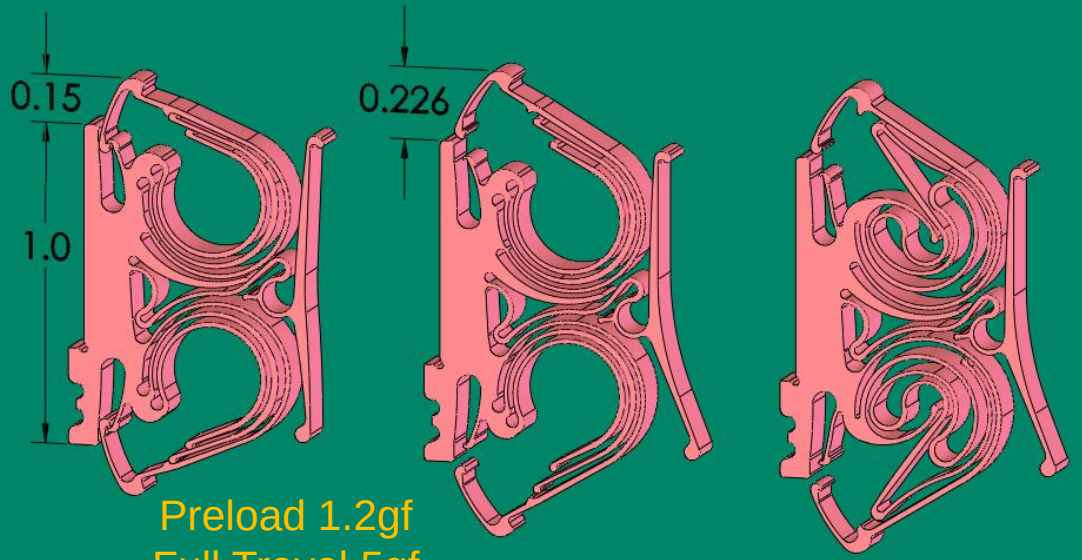
1.0mm Fully compressed Height

Total Travel is ~31% of Height

Targeted applications:
MLC, MLO to PCB
PCB-PCB
Test Sockets
OEM Sockets





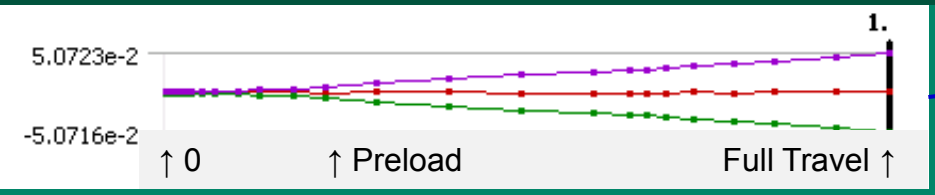


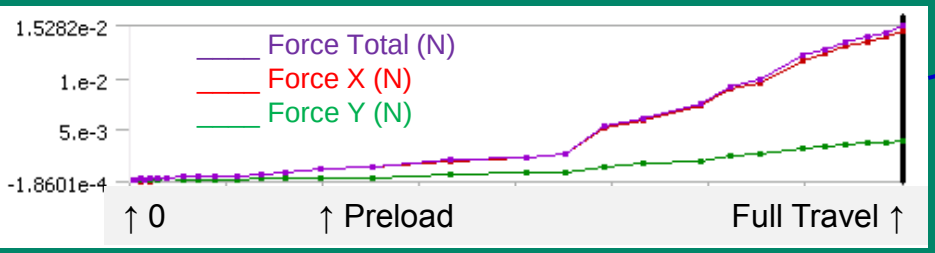
Preload 1.2gf
Full Travel 5gf
Low Force Version

High Force Version

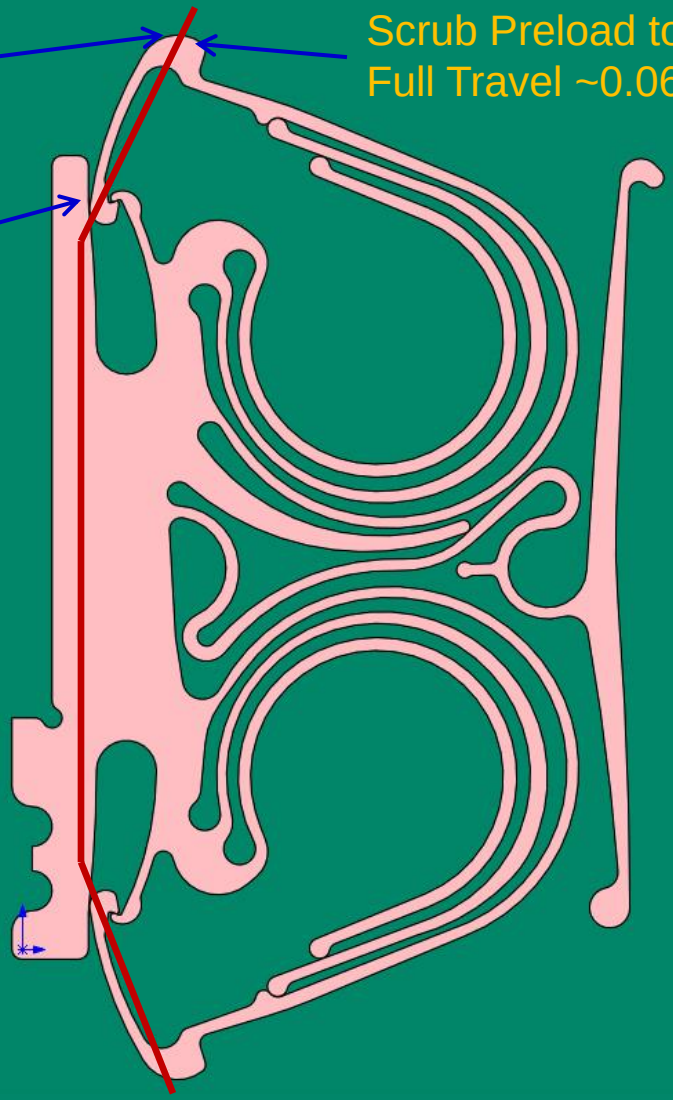
Dimensions in mm

0.8mm Pitch Interposer Array

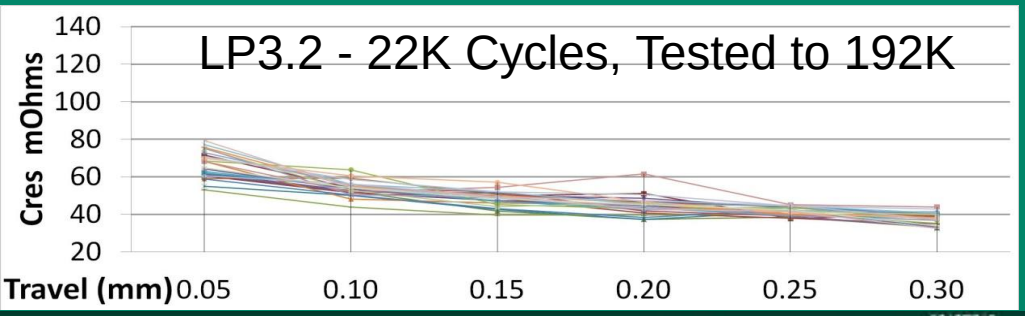


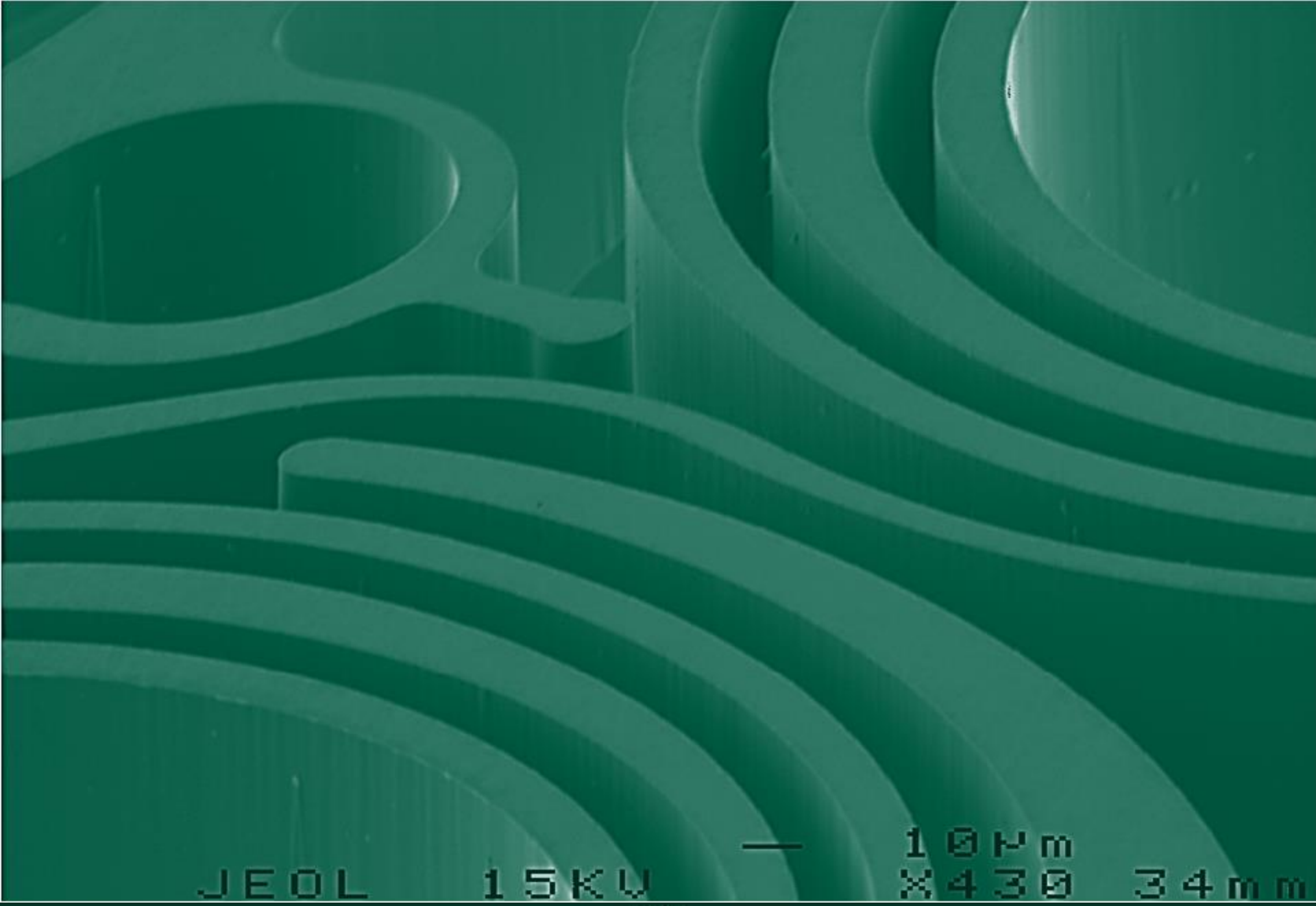


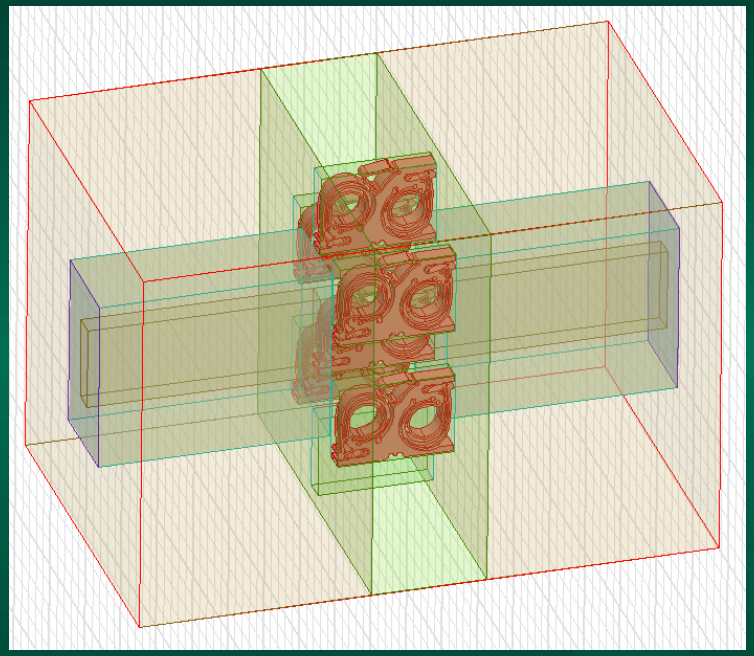
Scrub Preload to
Full Travel ~0.065mm



Design Goals
- Low Force √
- Short/Direct Signal Path √
- Scrub/Wipe at Contact Surfaces √
- Low & Consistence CRES √ *
- Low Cost √ *
- Well Suited for HVM Automation



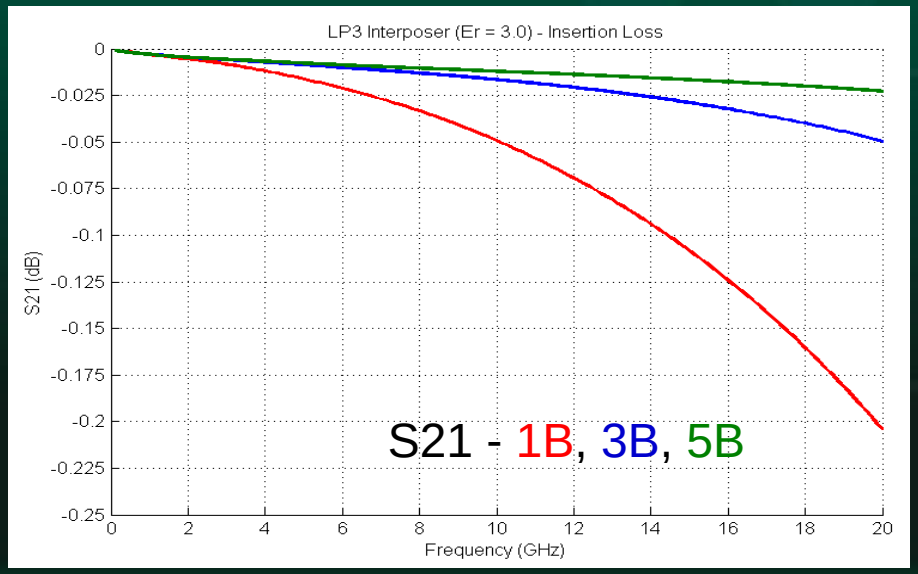

10μm
JEOL 15KU X430 34mm

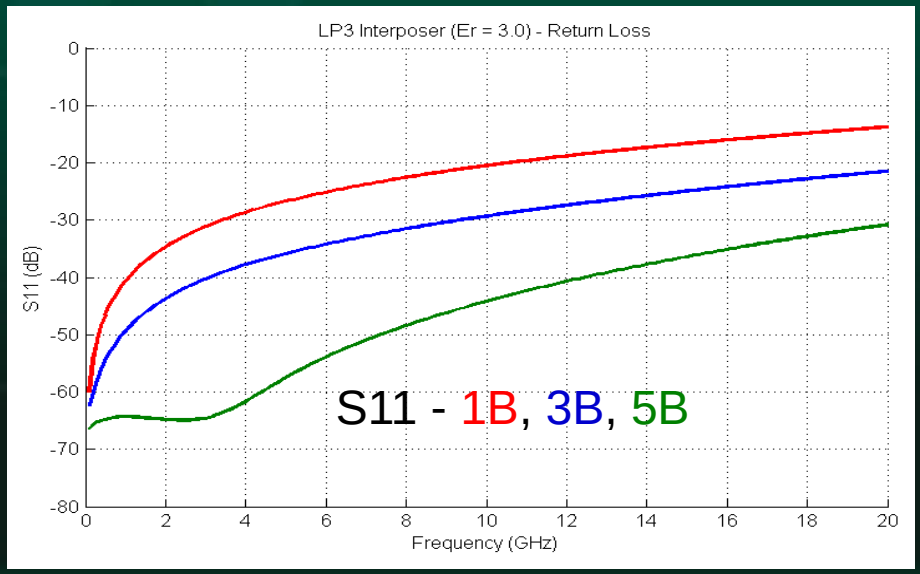


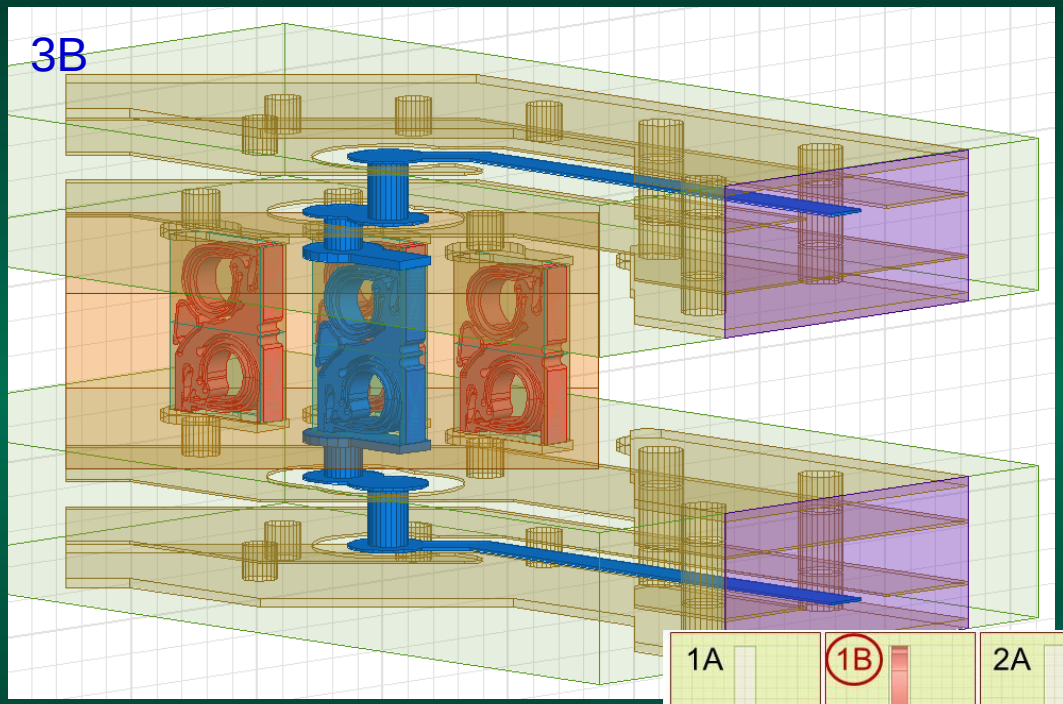
0.8mm Array Interposer Interconnect

The simulated SI data shown is in keeping with the standard industry practice of providing interconnect performance in use cases that can never be achieved by the end user in actual applications.

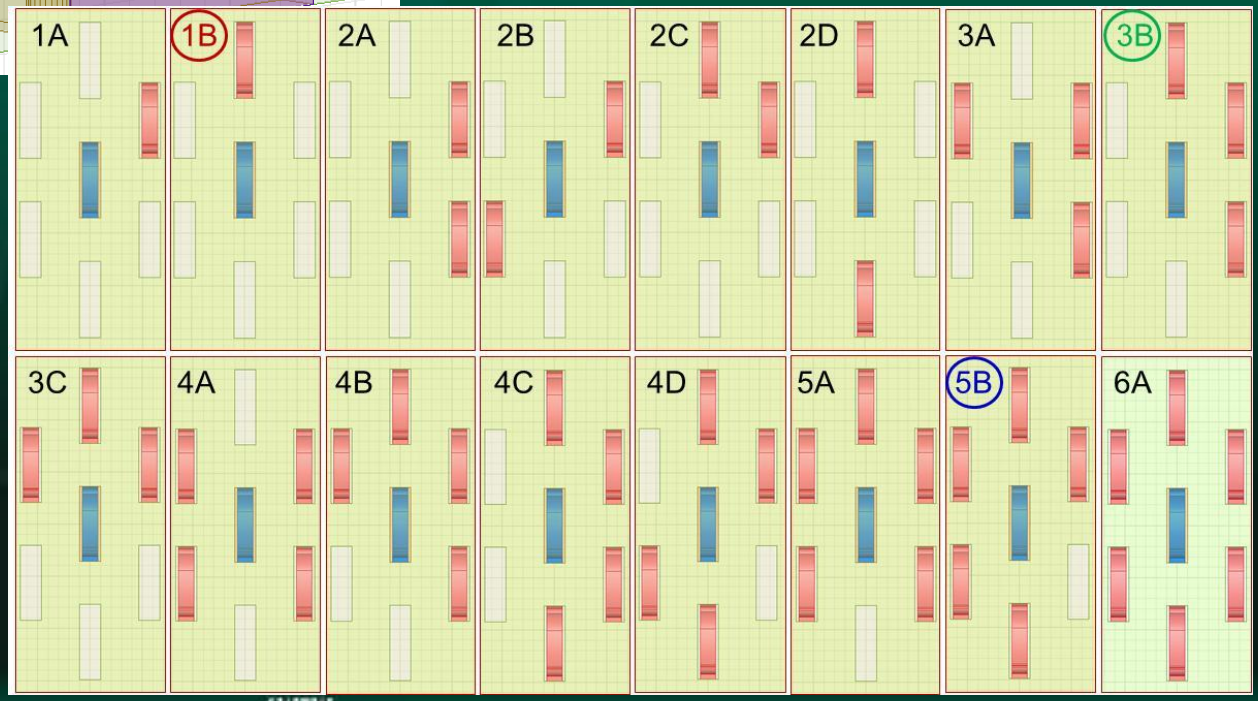
However in all fairness…



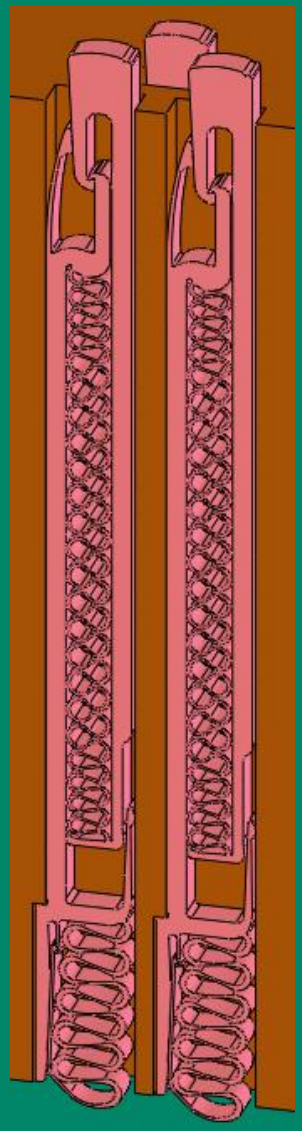


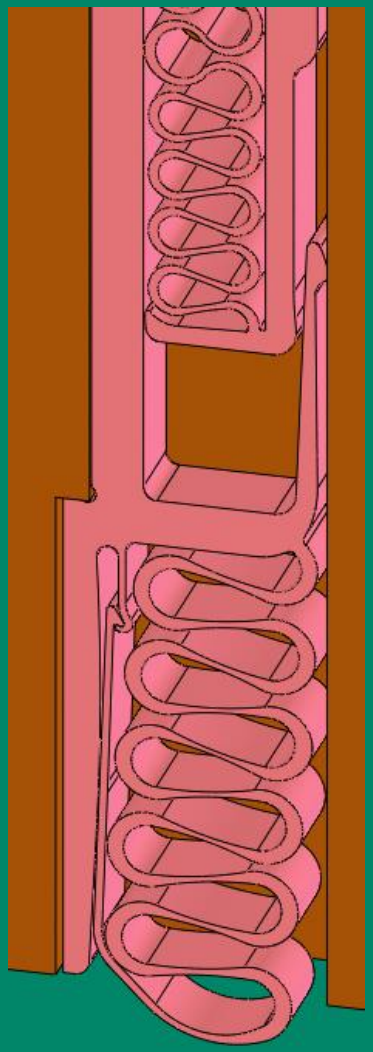


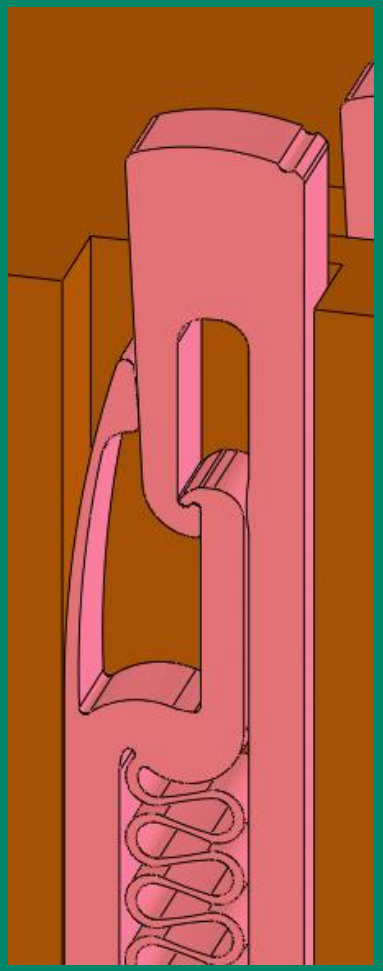
0.8mm Array



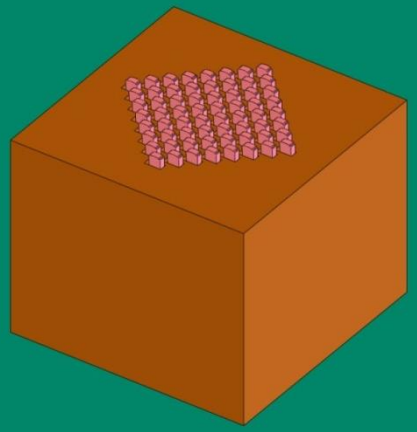
WLCSP-CSP Interconnects (0.4 mm Shown)

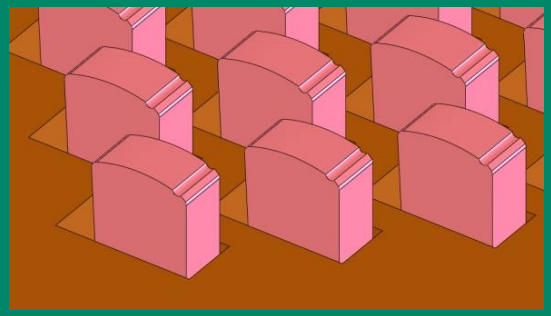




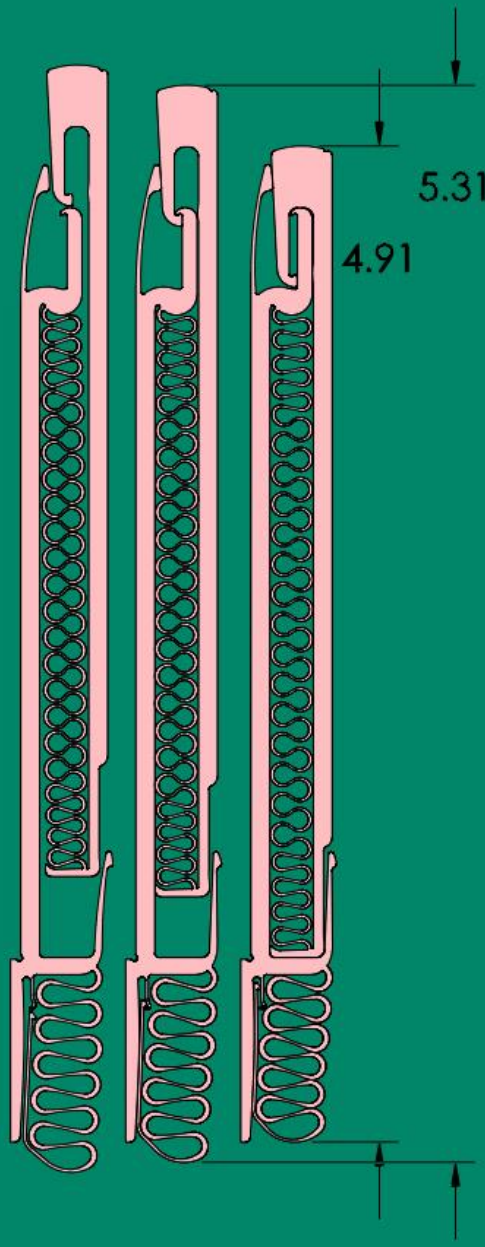


Design Goals
Low Force
Direct Signal Path
Scrub/Wipe at DUT Contact Surface
Low & Consistent CRES
Low Cost
HVM Automation
Array Pitches
- 0.8mm
- 0.4mm
- 0.3mm
- 0.2mm

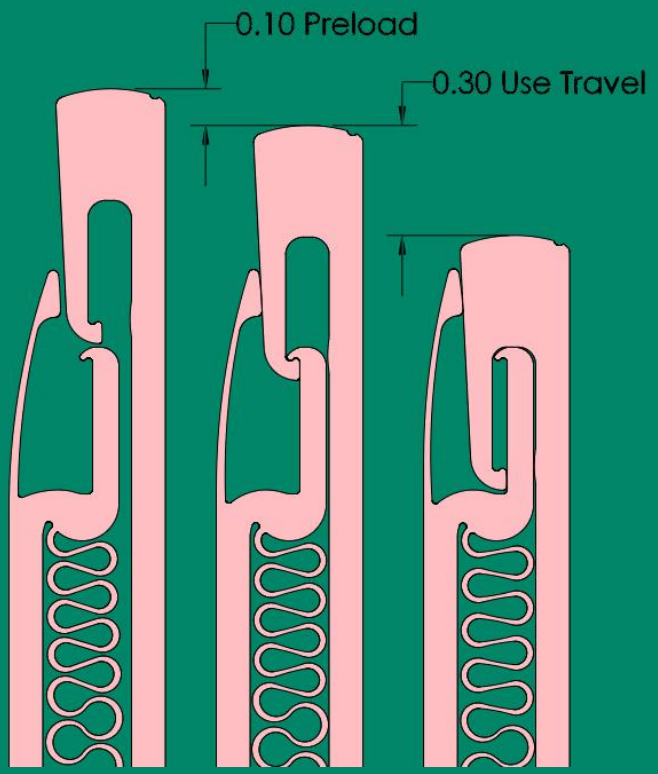


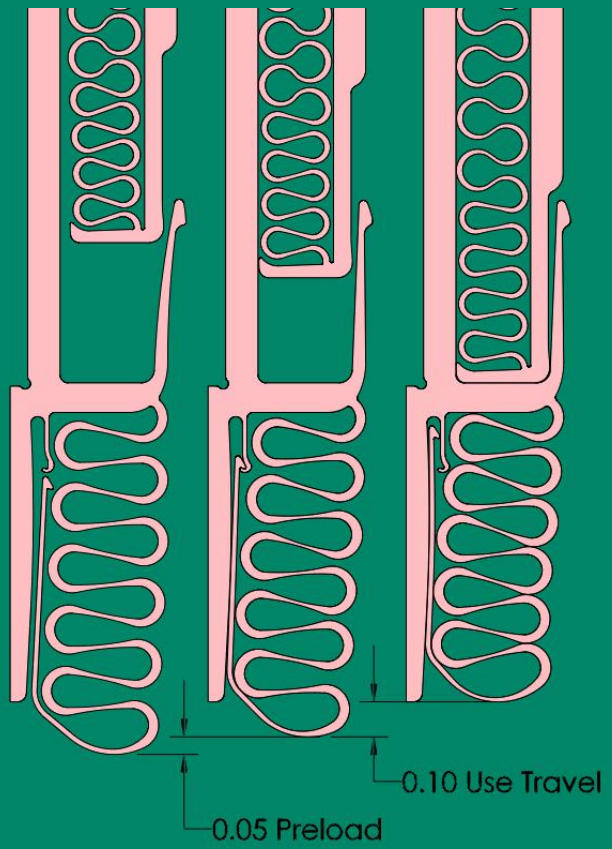


WLCSP-CSP Interconnects (0.4 mm Shown)



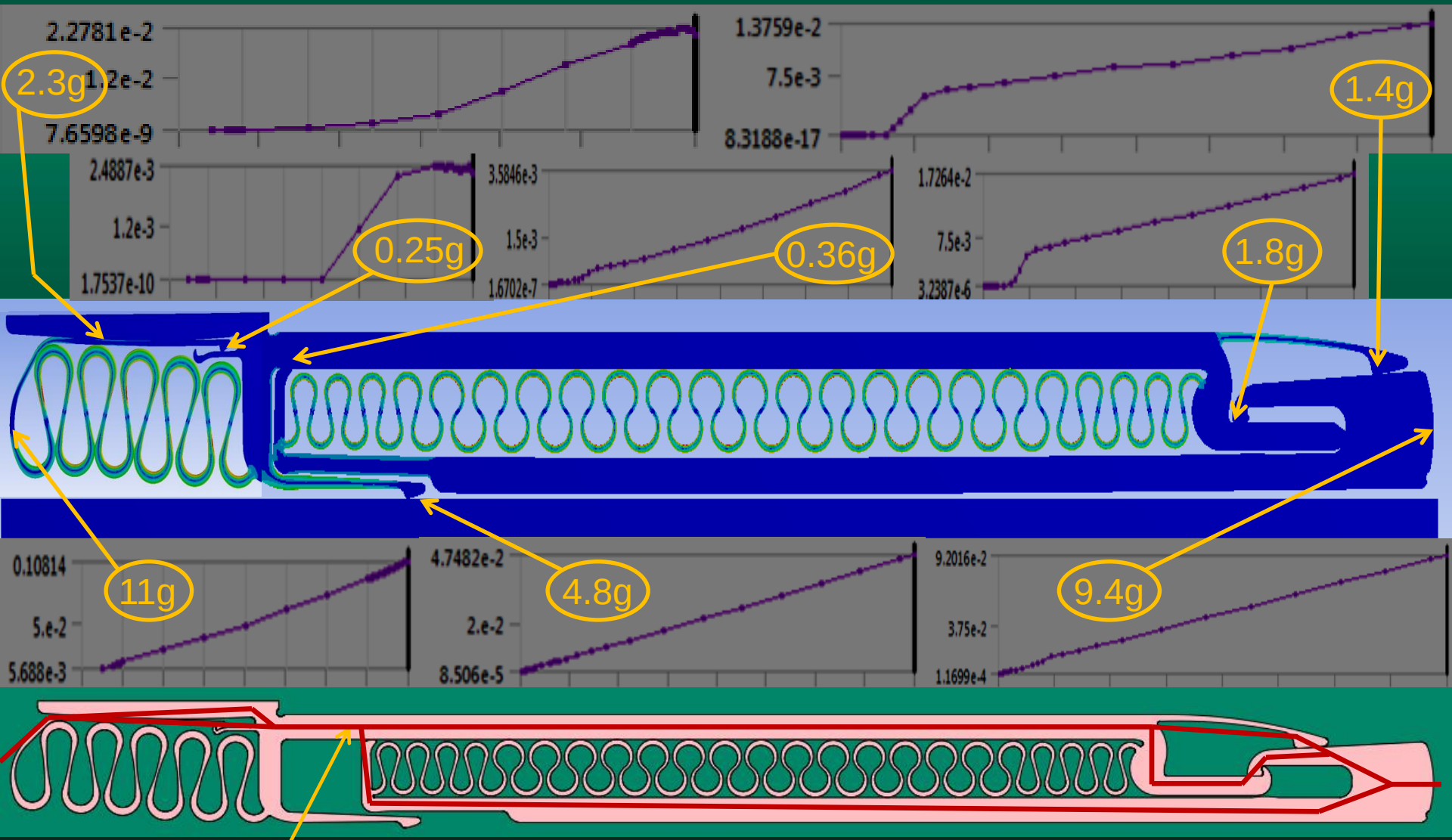
Preloaded 2.2gf, Full Travel 9.4gf





Preloaded 1gf, Full Travel 11gf

WLCSP-CSP Interconnects (0.4 mm Shown)



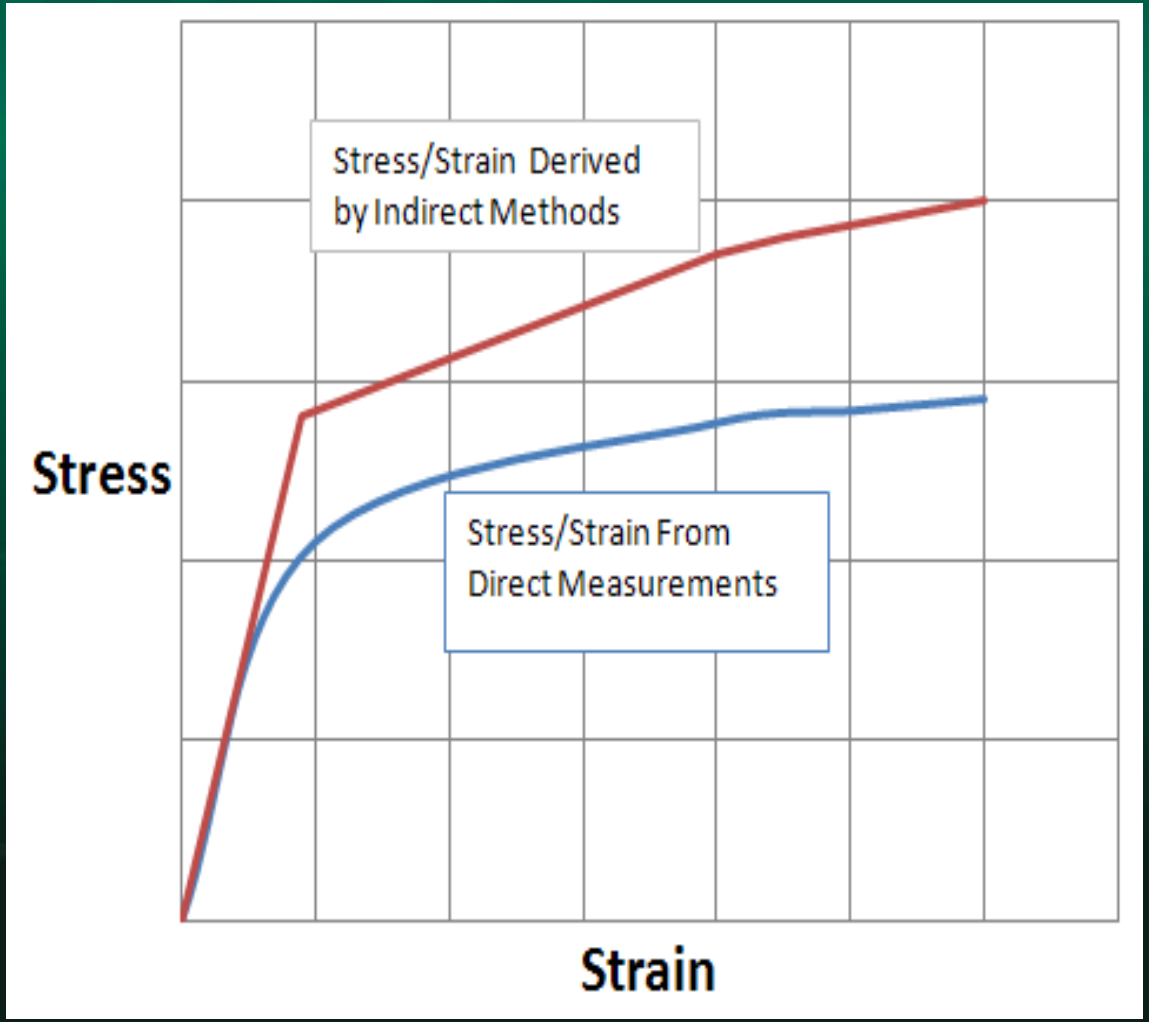
Material Properties Expectations Vs. Reality

Common industry (LIGA) practice is for mechanical properties to be indirectly derived from failure data.

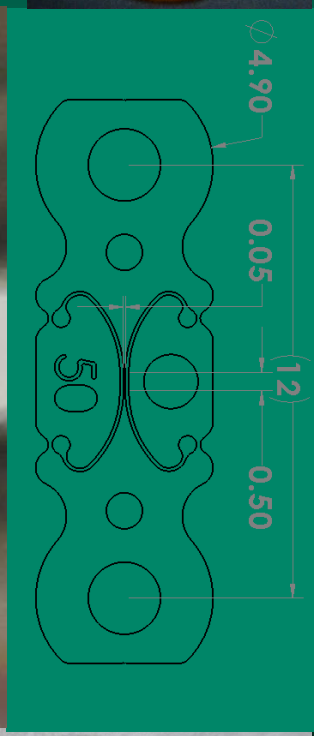
Current mechanical properties based on actual tests of micro samples.

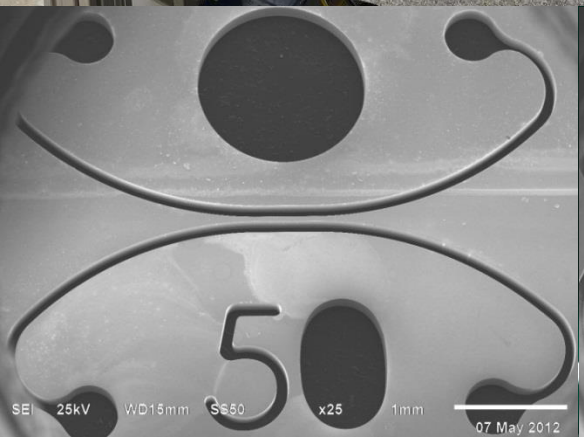
Precise Yield stress is difficult to define.

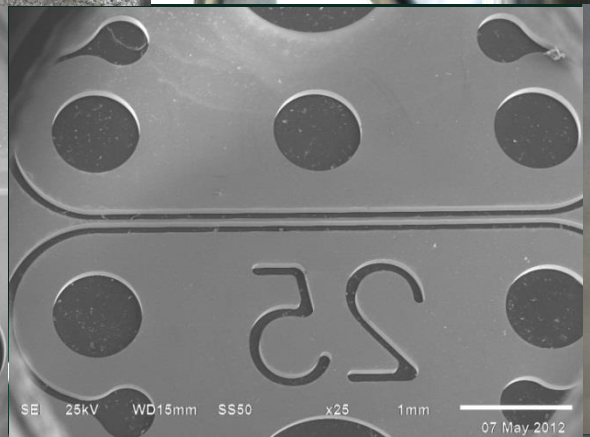
There is no substitute for direct measurements…

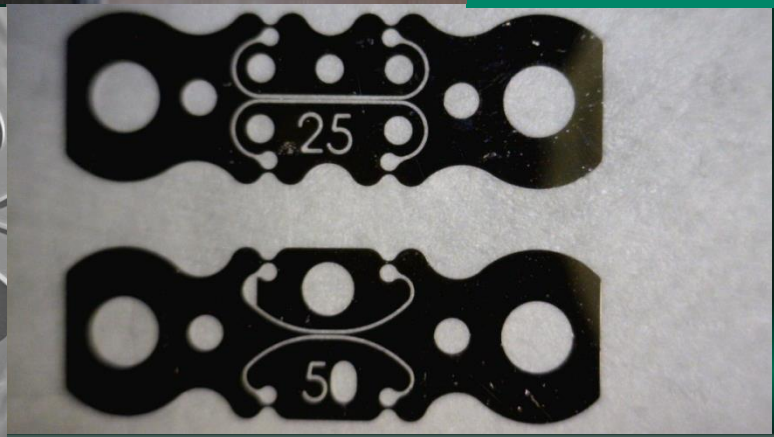


Material Properties
The solution







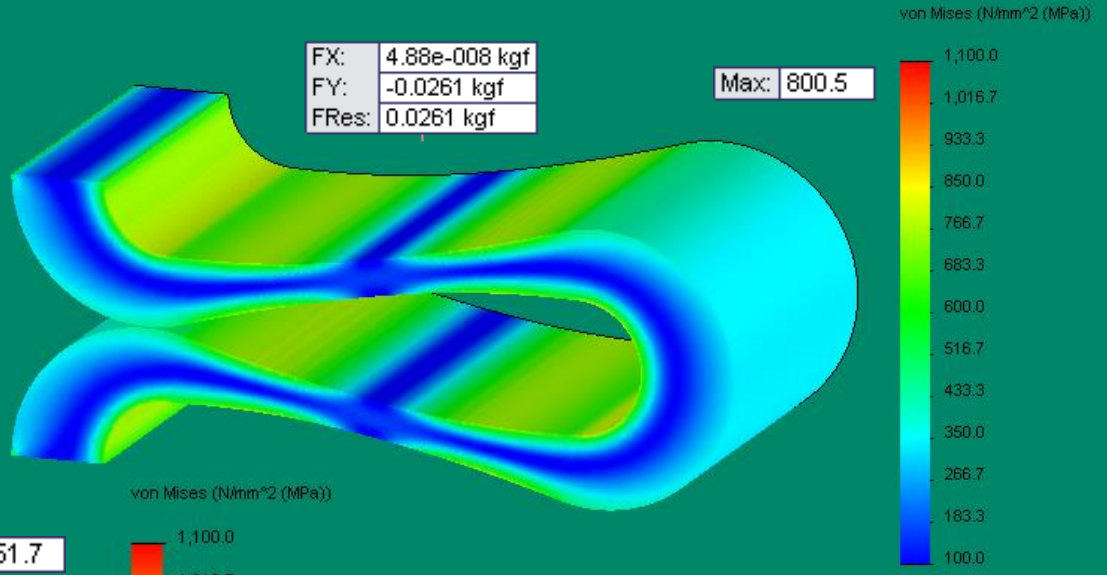


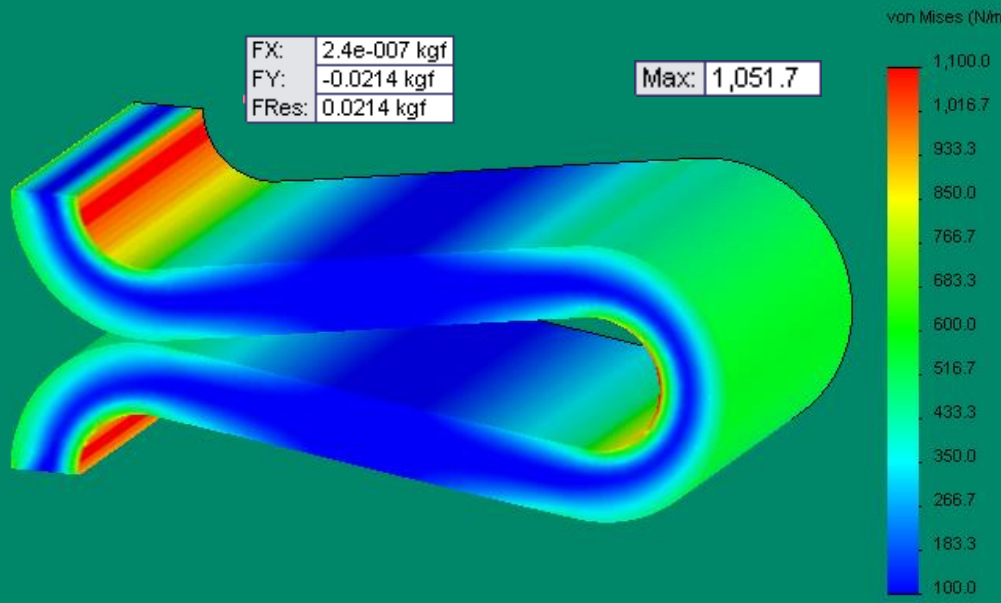
Design Advantages: Energy Storage

Allows for very efficient distribution and increased storage of strain energy

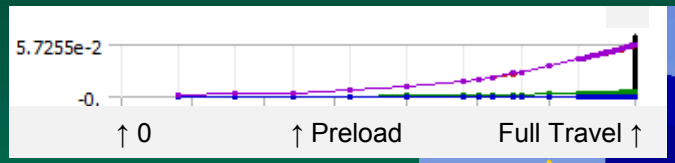
This example shows ~23% less peak stress with ~22% more force

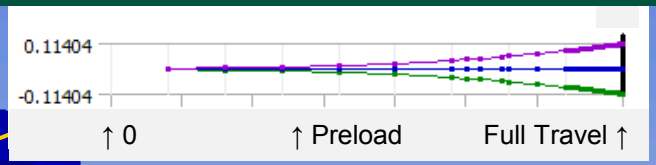
The only change is the tapering





Design Advantages: Flexibility





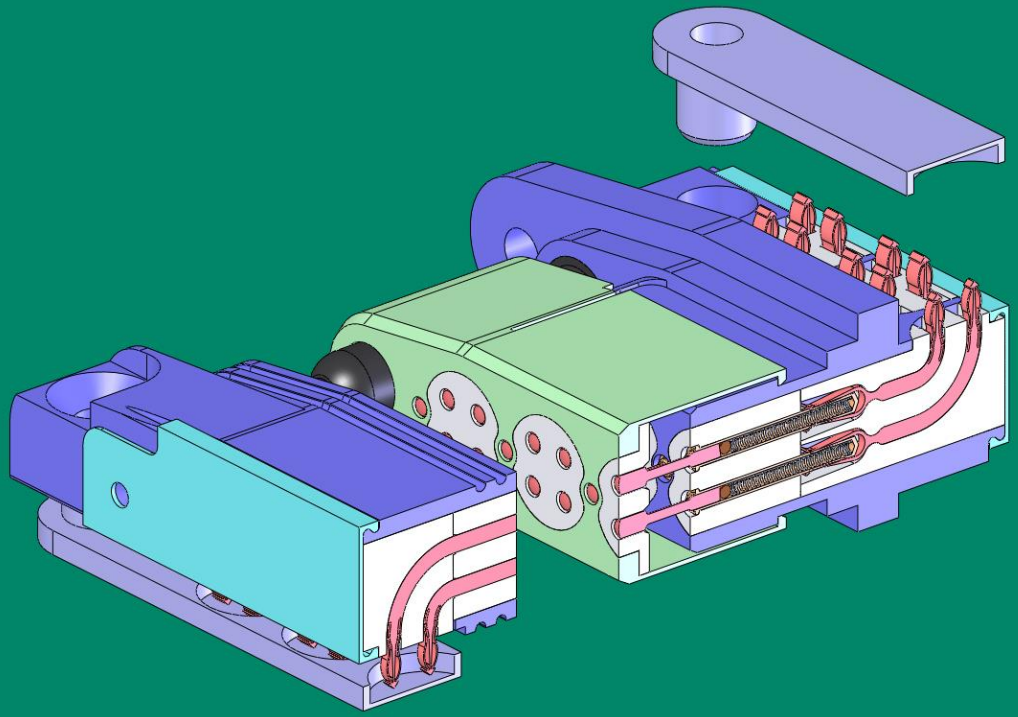

ANSYS
14.0

What's Important

(The critical links in the chain)

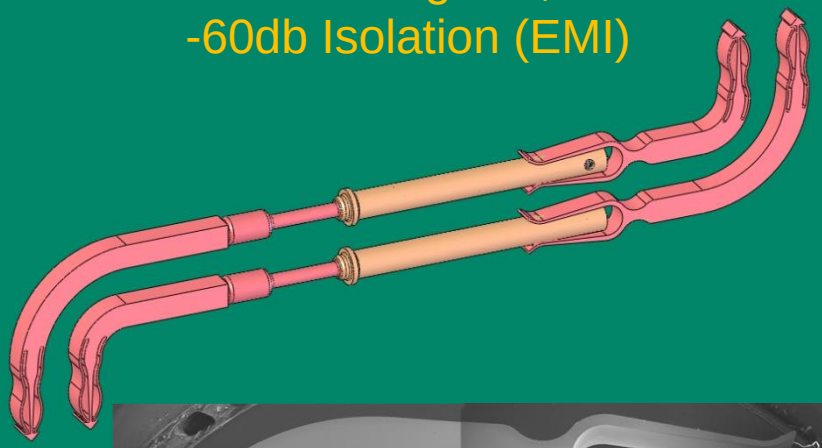
- Material Behavior
- Design Rules
- Process Knowledge & Stability
- Imagination
- ~~Preconceived notions~~

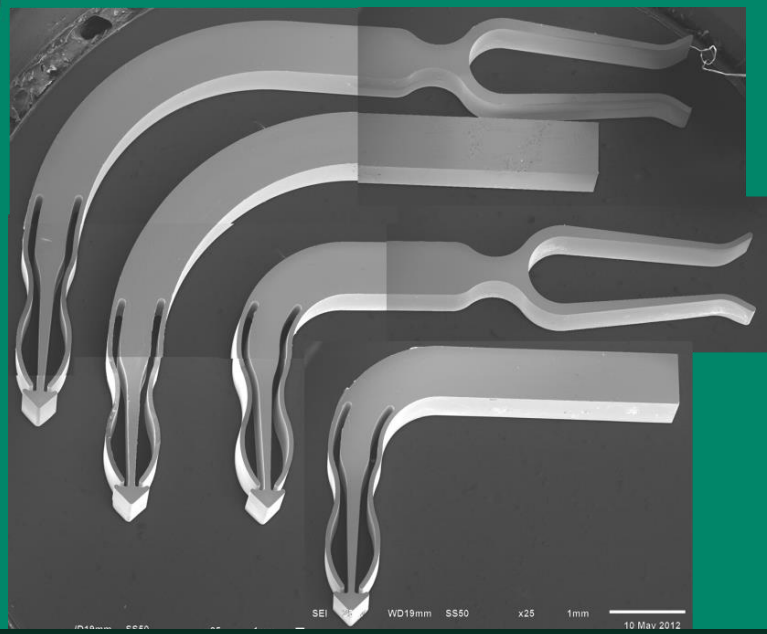
Design Advantages Prototype Flexibility

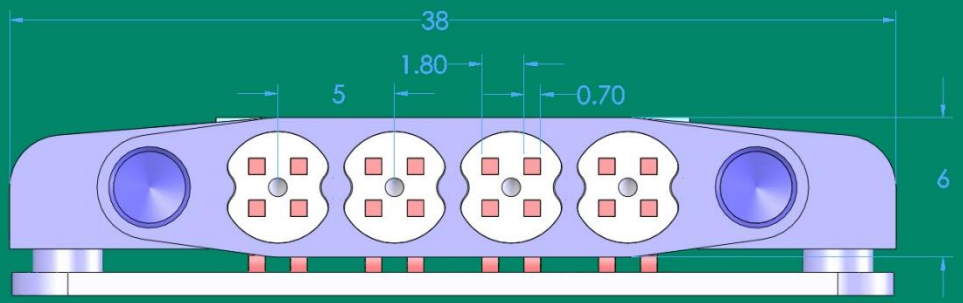


An effective Prototype Process

HDMI & USB 3.0 Signals, and Power
-60db Isolation (EMI)





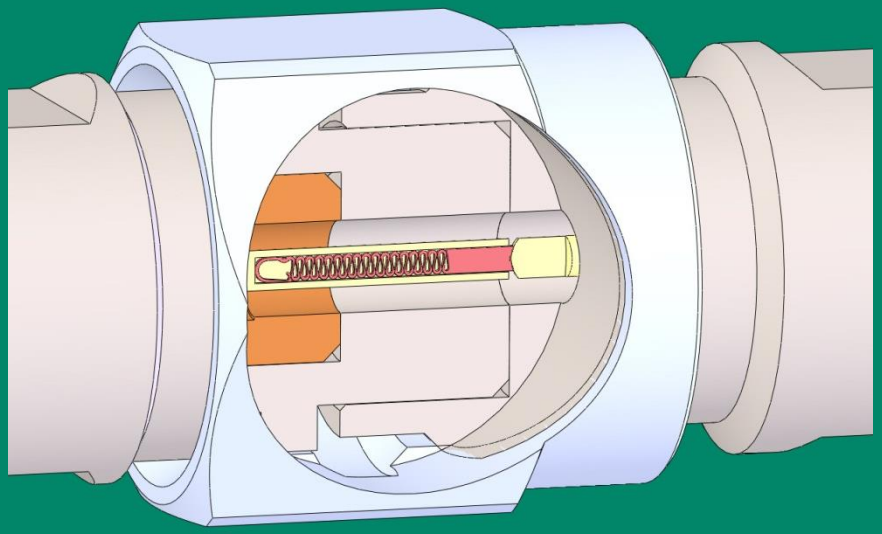


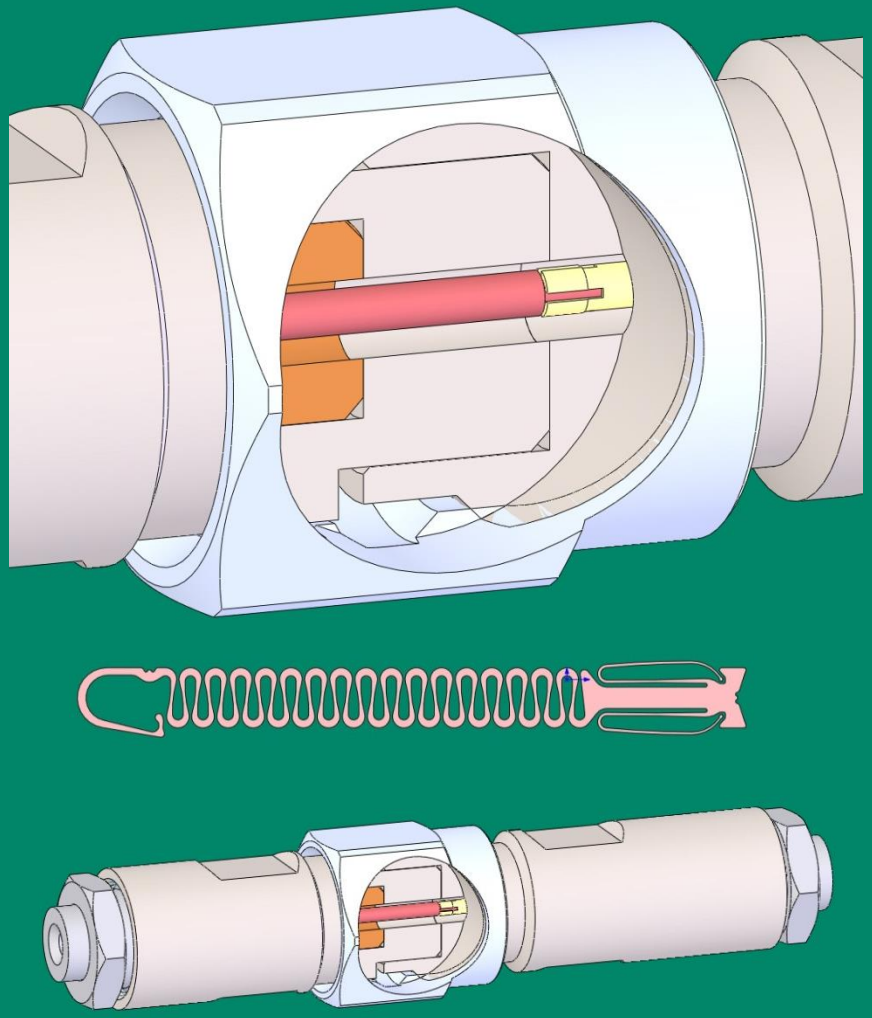
Dimensions in mm

What if…, Could we…

RPC-1.60 80Ghz Connector
Typical Pin & Socket Signal interconnect

Can we:
Improve the mating cycles -Yes
Improve the robustness -Yes
Improve the cost -Yes
Maintain the Signal Integrity - Close but No





- What's Next? (quite a bit)
  - Continued Reliability Testing & Characterization
  - Continued Signal Integrity Characterization
    - Beta Site Testing
  - Surface Platings
  - Layering materials
  - Commercialization
    - Consumables
    - OEM
    - 2nd source partnerships
      - Will we sell loose Interconnects? - yes

Please visit us in the exhibitor's area if you would like to discuss this further

Thank you for your time

Appendix

Our Development Team

Bernhard Rosenberger CTO, Head of WW R&D (Germany)

Dr. Michael Wollitzer, Head of R&D (Germany)

Jim Jaquette MCI Program Manager (USA)

Roland Neuhauser MCI Project Manager, Factory liaison (Germany)

Steve Fahrner MCI Structual, Thermal, Material Analysist (USA)

Trevor Mitchell MCI Signal Integrity Engineer (Germany)

Michael Angerbauer Materials Test Engineer (Germany)

Florian Wohlschlager Reliabitily Test Engineer (Germany)

Frank Schonig MCI Designer, R&D (USA)

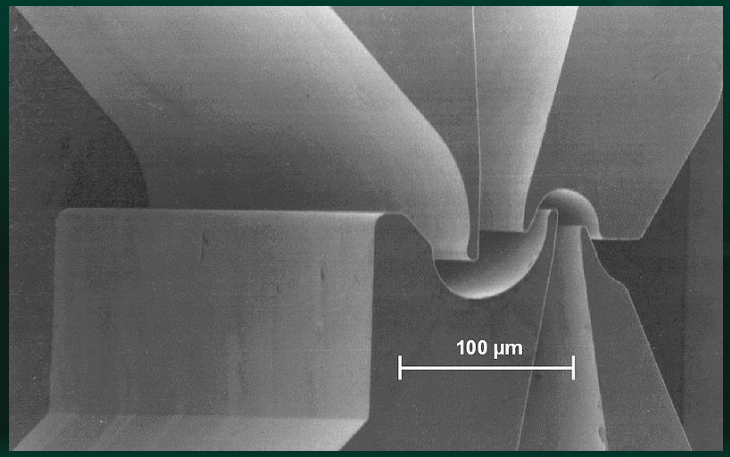
Hauke Schütt Business Unit Manager Test and Measurement (Germany)

Hans Rosenberger CEO (Germany) (The guy that pays for all this)

The LIGA Process

LIGA is a German acronym for: *Lithographie, Galvanoformung, Abformung* (Lithography, Electroplating, and Molding) a fabrication technology used to create high-aspect-ratio microstructures.

- X-Ray LIGA is a fabrication process in micro-technology that was developed in the early 1980s.
- X-Ray LIGA requires exposure to parallel beams of high-energy synchrotron radiation (X-rays)
- UV LIGA utilizes an inexpensive ultraviolet light source
- UV LIGA is much cheaper and more accessible than its X-ray counterpart.
- UV LIGA is not as effective at producing precision molds as its X-ray counterpart.
- UV LIGA is used when cost must be kept low and very high aspect ratios are not required.



The X-ray LIGA process was originally developed at the Forschungszentrum Karlsruhe, Germany, to produce nozzles for uranium enrichment.

http://en.wikipedia.org/wiki/LIGA

LIGA X-Ray & UV Comparative Pros & Cons

- X-Ray LIGA Pros
  - Extremely high aspect ratios 100:1
  - Less processing risks compared to UV
  - Cost efficient for wide range of Prototyping projects
- X-Ray LIGA Cons
  - limitations in beam width, practically speaking 4” wafers max (leads to misconception on cost)
  - Availability to synchrotron beams limited to universities and government facilities
  - Synchrotron beams require noteworthy down time due to maintenance, both scheduled, and non-scheduled
- UV LIGA Pros
  - Currently available on 6” & 8” wafers (as with IC’s it’s a real estate business)
  - Δ in Precision is in the Nano-meter range when compared to X-Ray
  - Aspect ratios so far are not viewed as limitations
  - Significantly less costly than other currently available and well know competing processes
- UV LIGA Cons
  - Difficult to layer, generally accepted limit is 3 layers (thickness is not limited)

Where it all started for us

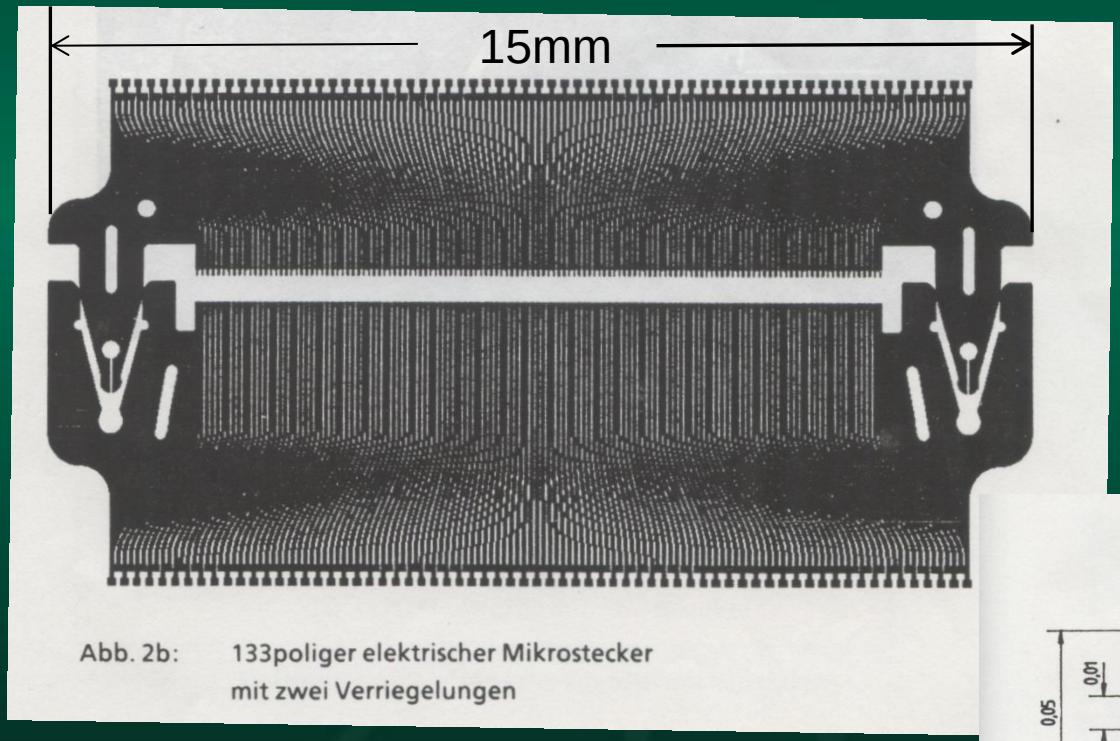


Abb. 2b: 133poliger elektrischer Mikrostecker mit zwei Verriegelungen

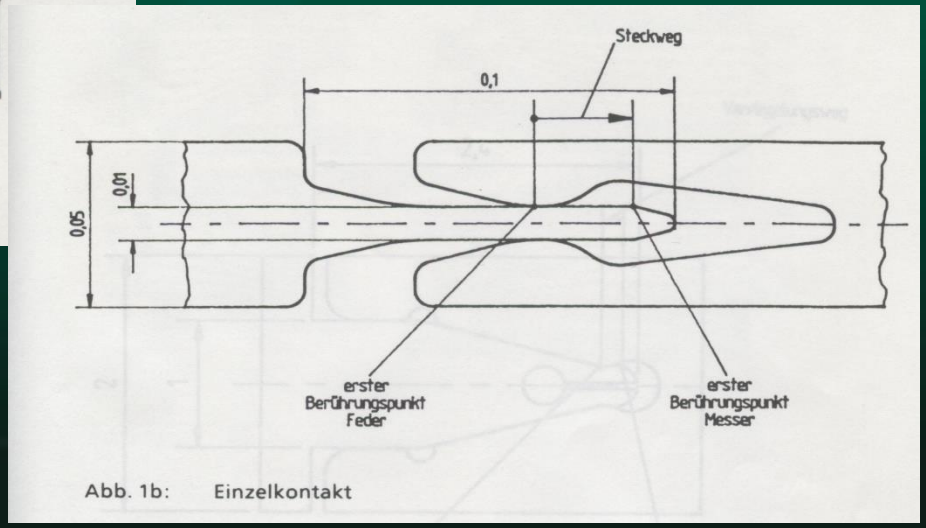


Abb. 1b: Einzelkontakt

1991 Rosenberger, the German Government, and Forschungszentrum Karlsruhe, Germany

Dimensions in mm