LIGA

Precision Microfabrication for Electromechanical applications

Frank Schonig

Innovative Micro Design

2014 BiTS Workshop

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Outline

A short history of LIGA

LIGA the process

Commercialized LIGA Products

Interconnects and applications

Process advantages

Appendix

BiTS WORKSHOP

Landscape photo: Ben-Creative/iStock

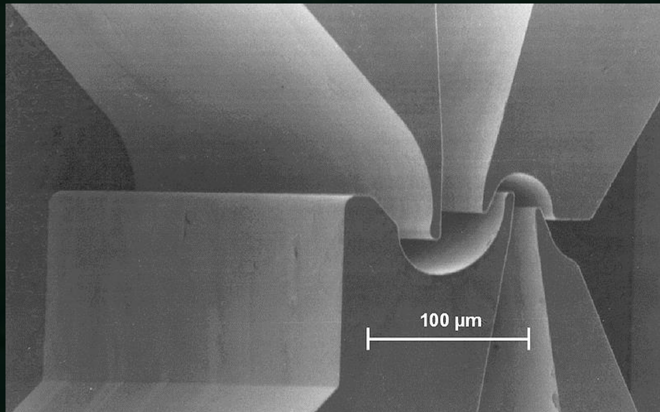
LIGA - Wikipedia

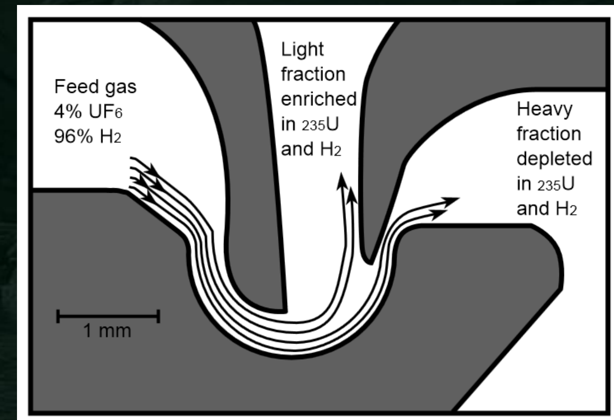
LIGA is a German acronym for: *Lithographie, Galvanoformung, Abformung*

(Lithography, Electroplating, and Molding) a fabrication technology used to create high-aspect-ratio microstructures.

- X-Ray LIGA is a fabrication process in micro-technology that was developed in the early 1980s.
- X-Ray LIGA requires exposure to parallel beams of high-energy synchrotron radiation (X-rays)
- UV LIGA utilizes an inexpensive ultraviolet light source
- UV LIGA is much cheaper and more accessible than its X-ray counterpart.
- UV LIGA is not as effective at producing precision molds as its X-ray counterpart.
- UV LIGA is used when cost must be kept low and very high aspect ratios are not required.

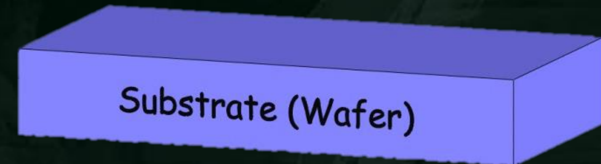
"The X-ray LIGA process was originally developed at the Forschungszentrum Karlsruhe, Germany, to produce nozzles for uranium enrichment". http://en.wikipedia.org/wiki/LIGA

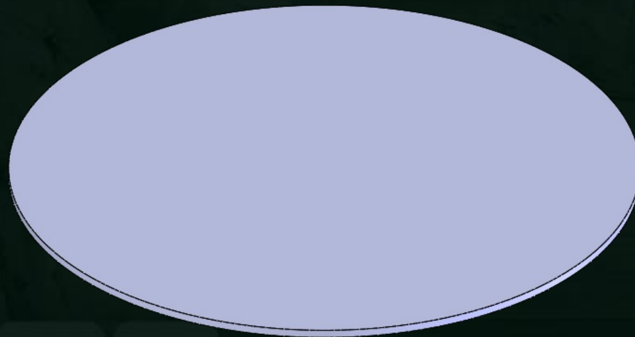




LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release





LIGA the process

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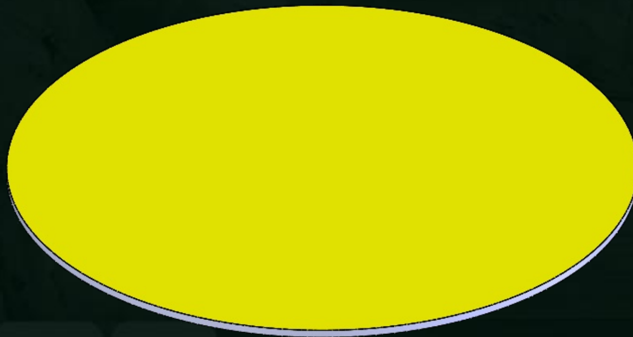
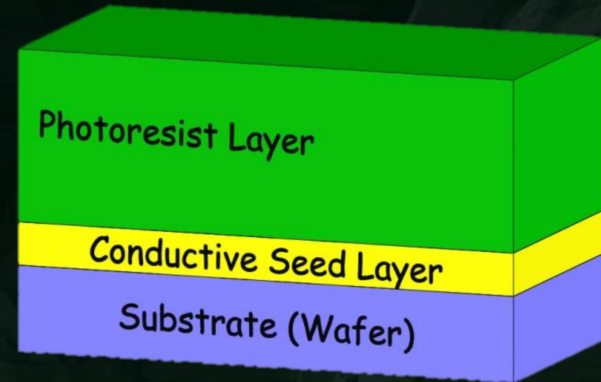


Conductive Seed Layer
Applied with PVD Process

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

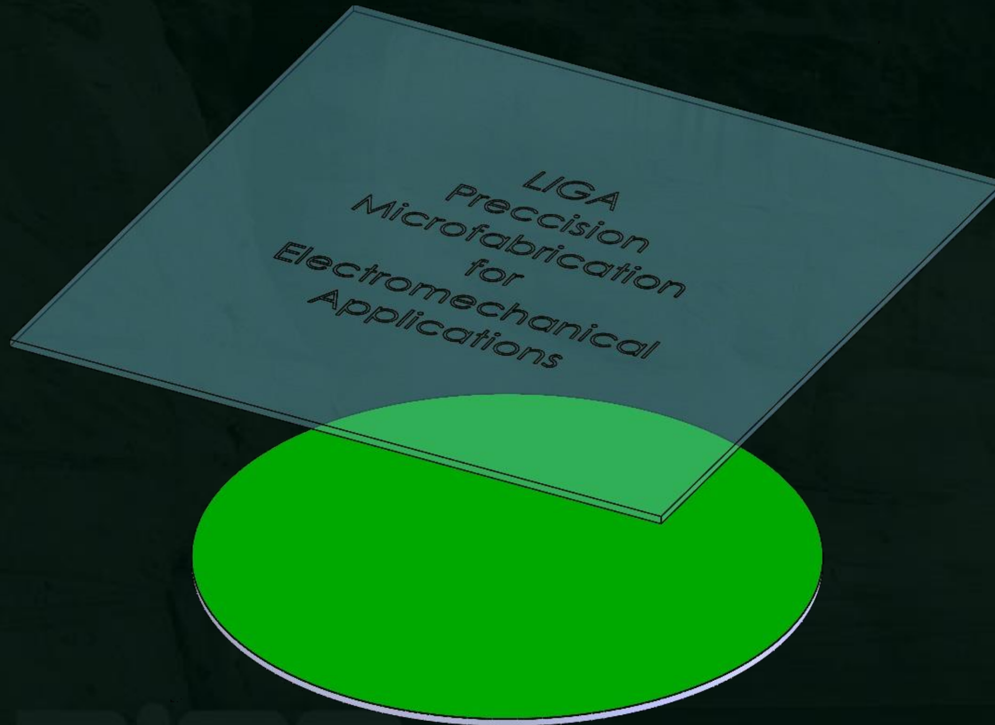


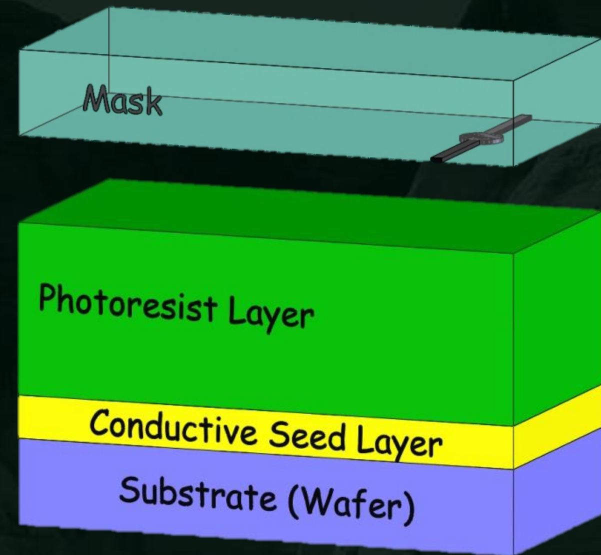
Photoresist applied with
Spin Coat Process

Wafer ready for processing

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

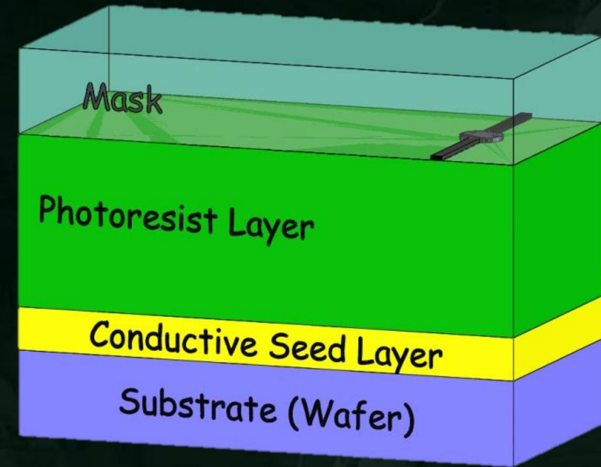


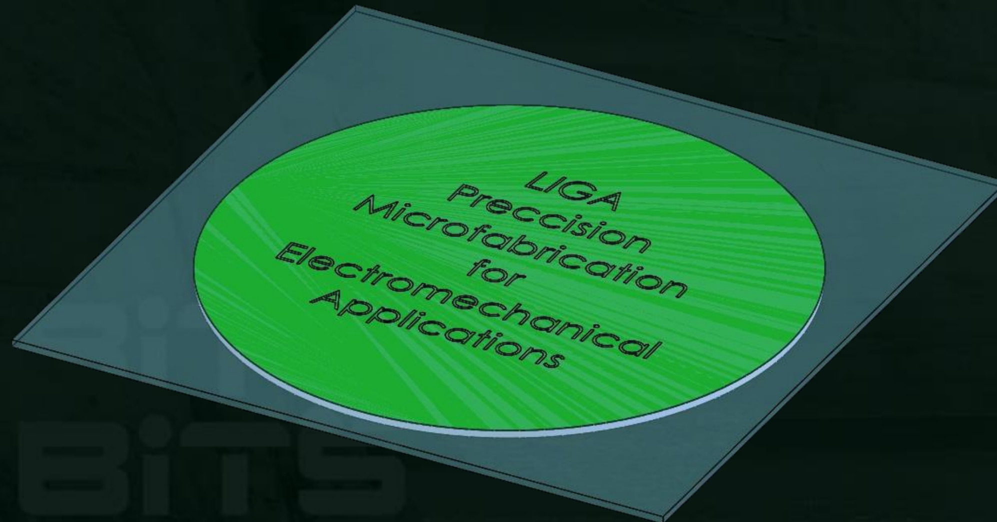


Design and Procure Mask

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

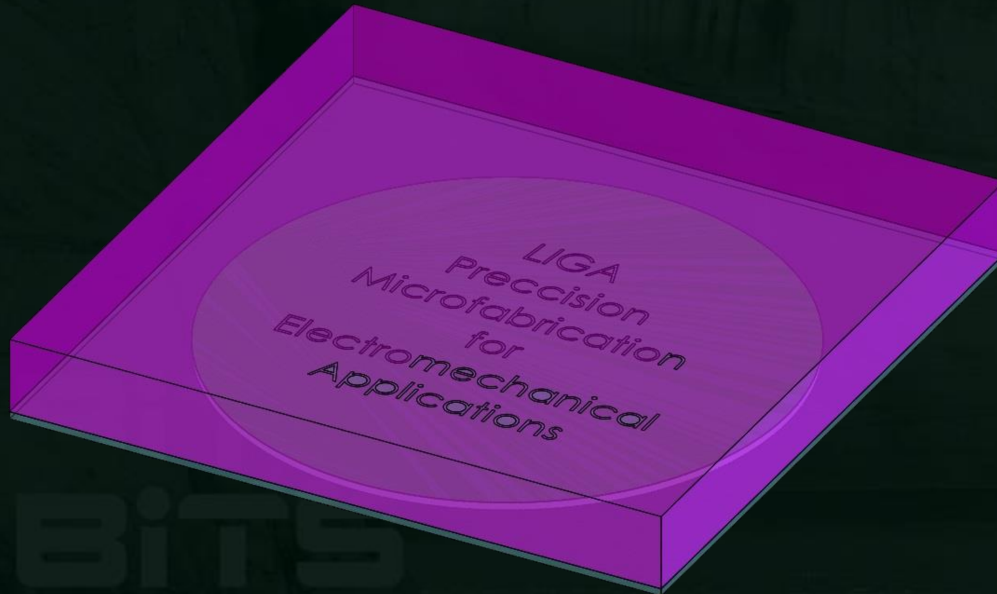


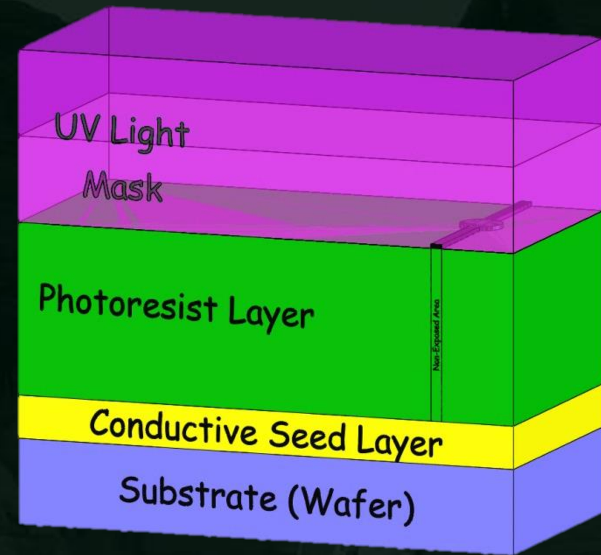


Mask is Aligned to Wafer

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

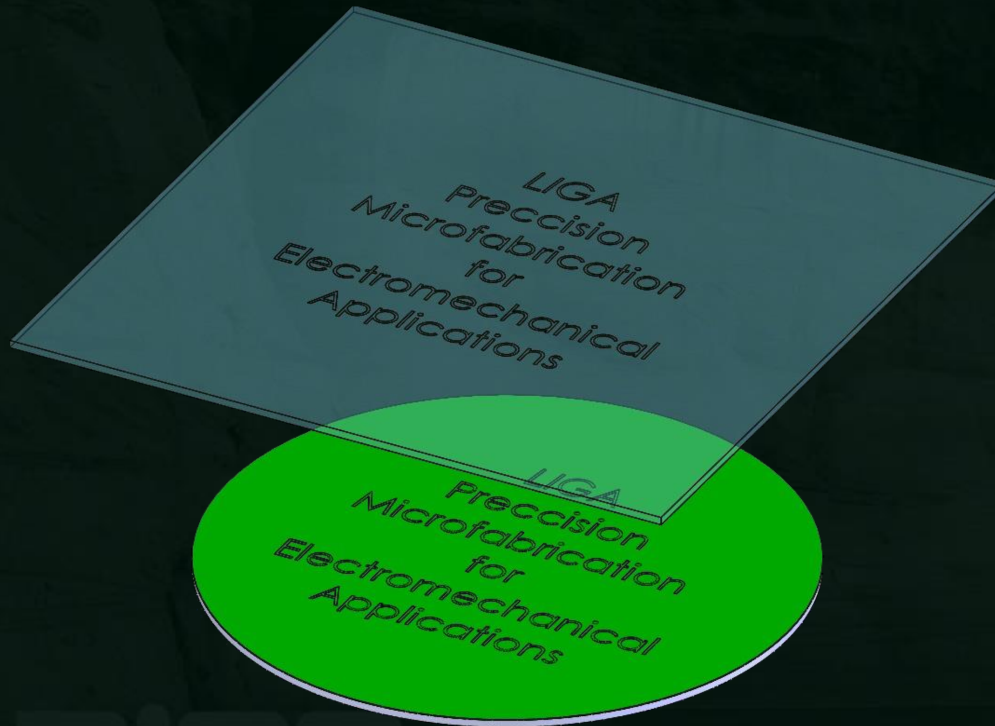


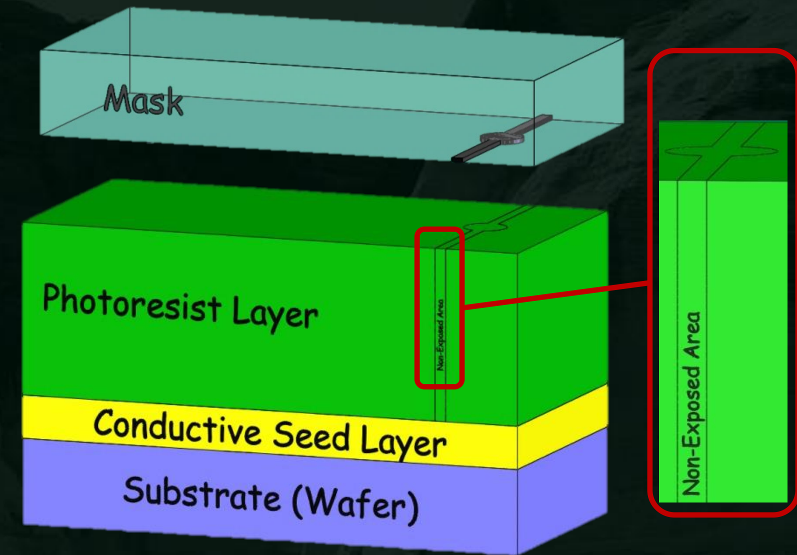


Exposed to a UV Light Source

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

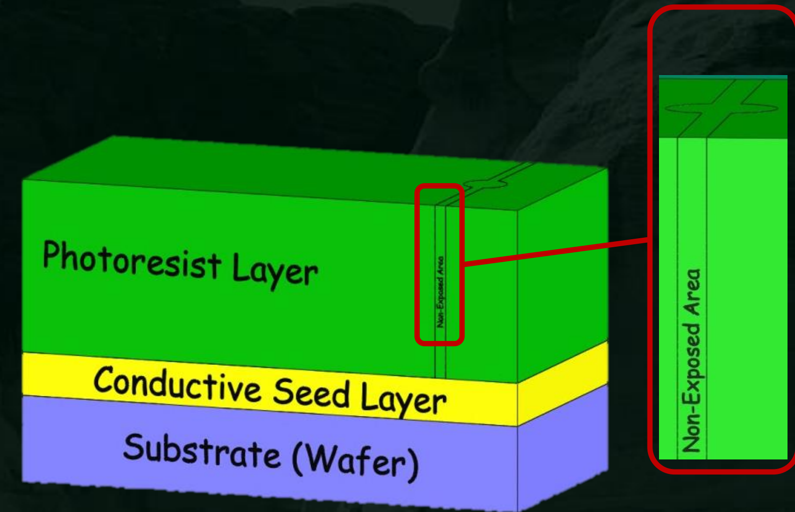




Mask Pattern is Transferred

LIGA the process

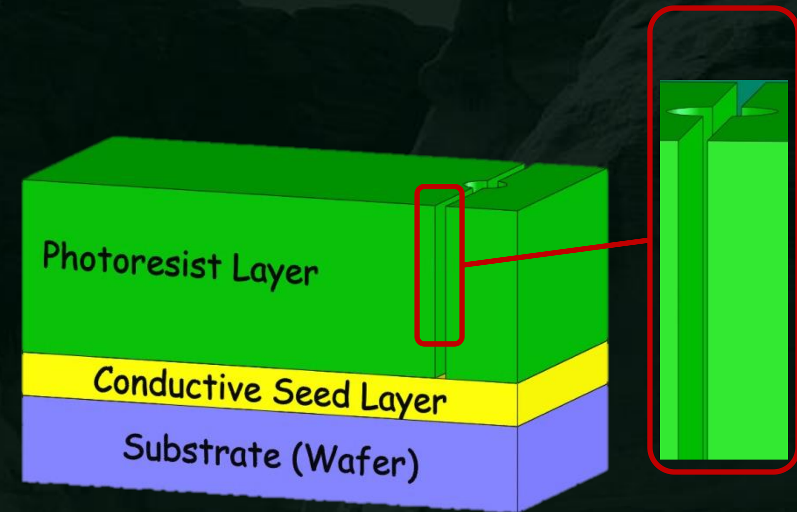
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

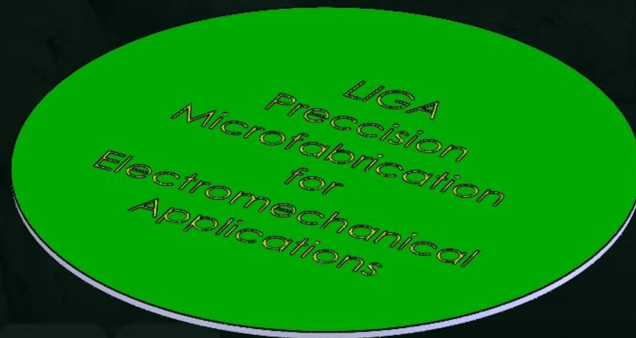


Photoresist Is cured
In Curing Process

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



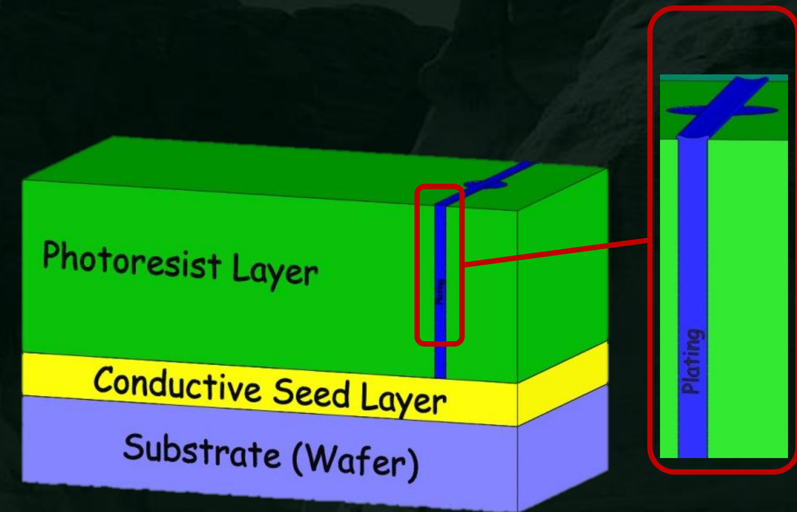


Non-Exposed Photoresist Chemically Remove
(Conductive layer now exposed)

Wafer can now be defined as a Mold

LIGA the process

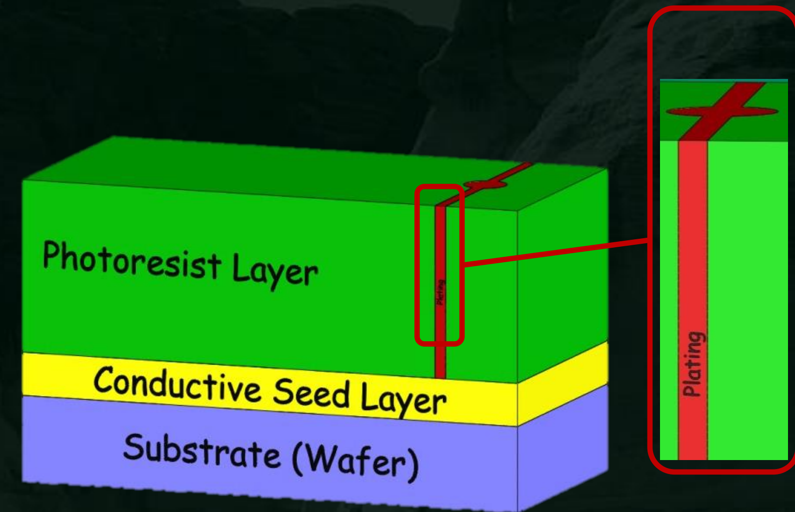
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



Wafer is Plated

LIGA the process

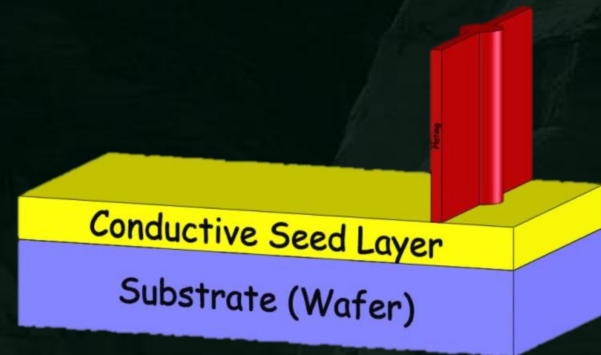
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release



Wafer is Lapped to final thickness

LIGA the process

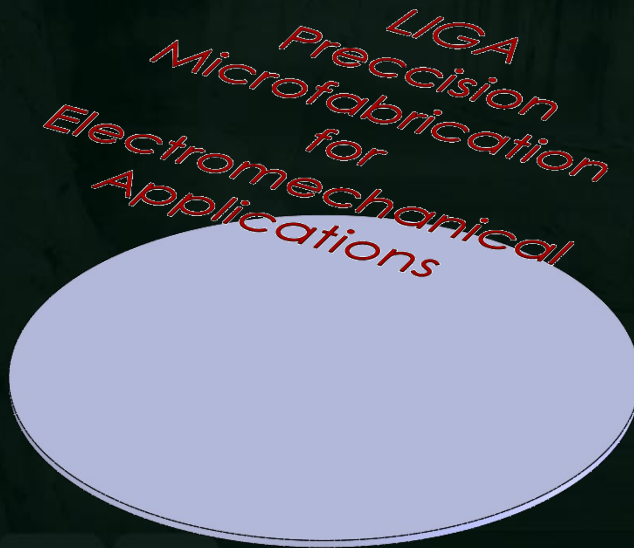
Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

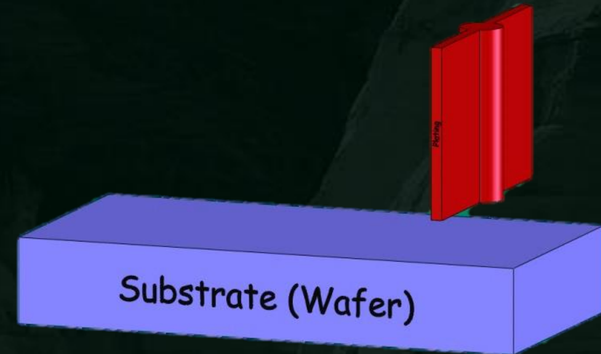


Photoresist Removed with Plasma Etch Process

LIGA the process

Wafer Prep → Exposure → Develop → Plating → Planarizing → Etch → Release

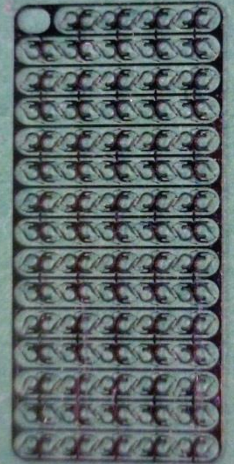


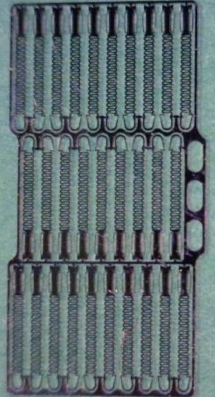


Conductive Seed Layer Chemically Removed

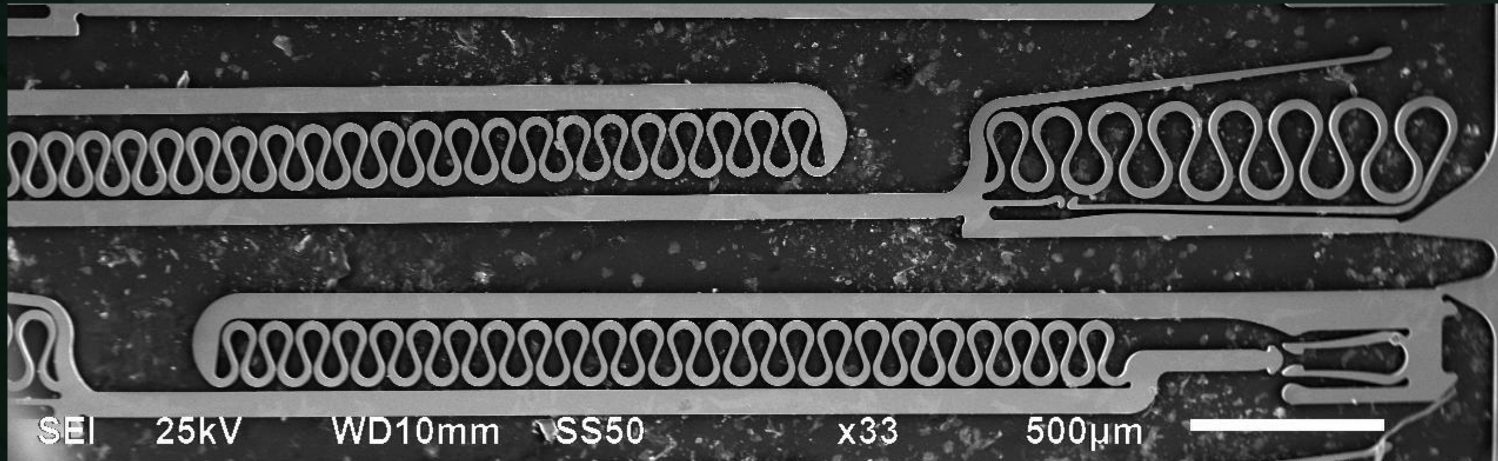
Parts are released

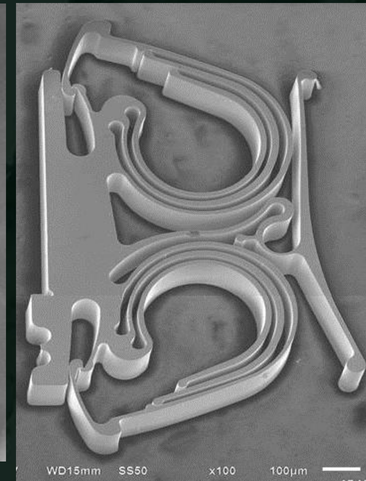
Example of released wafer

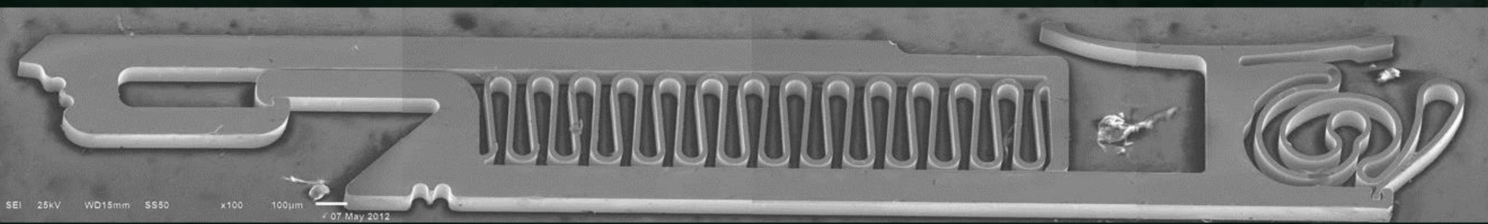


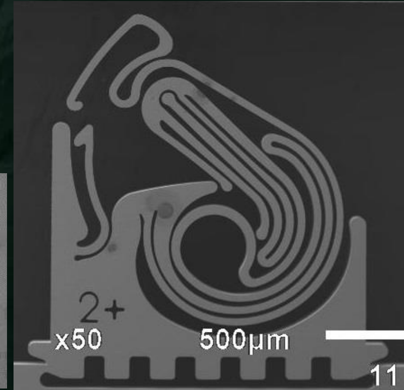


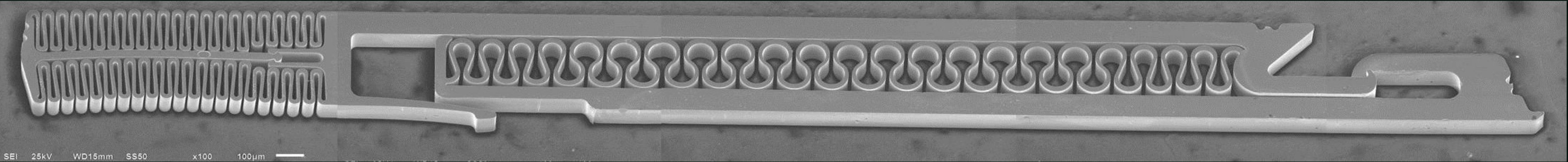
Interconnect Examples











Materials

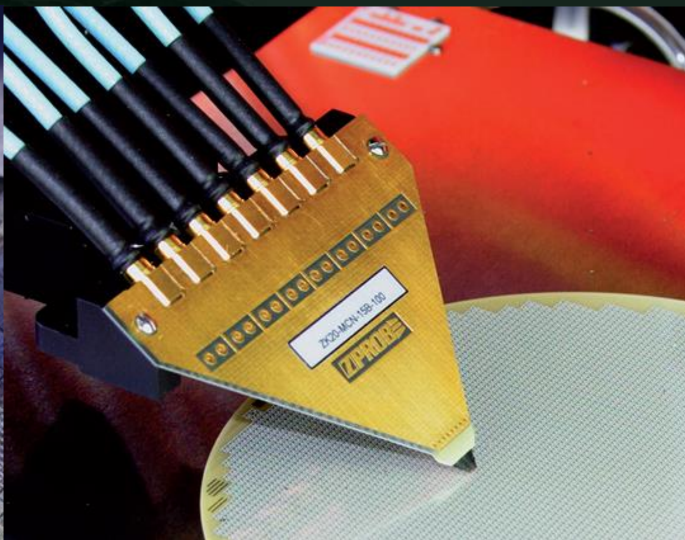
Electroform materials

Ni
NiCo
NiP
NiFe
NiW
Au
AuNi
AuCo
Cu
Ag
Others…

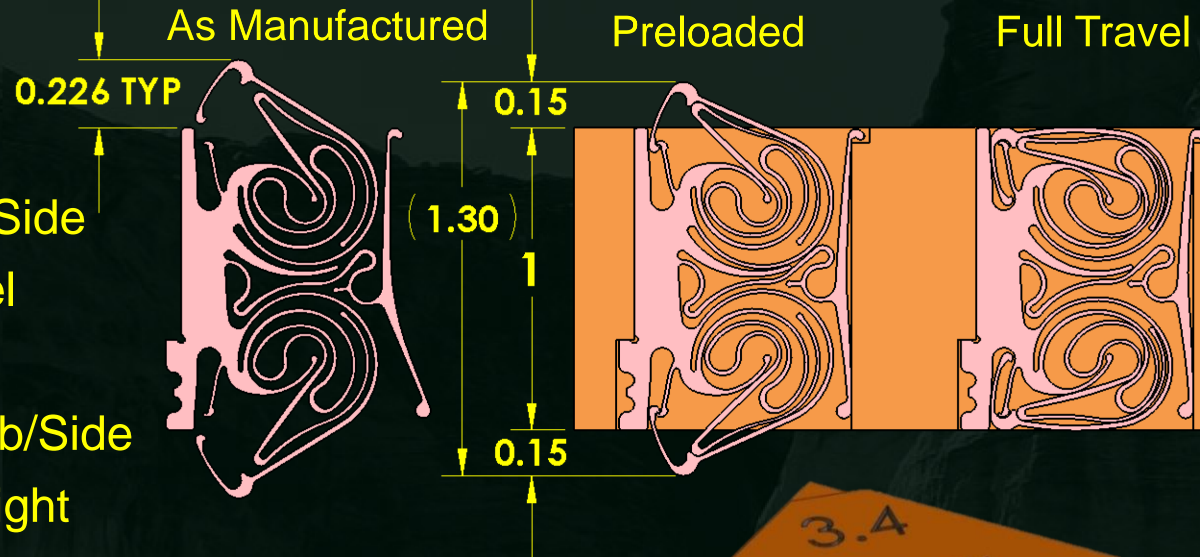
Electroplate only materials (<5µm)

Ru
Rh
Pd
W
And all of the Electroform list

Commercialized LIGA Products



0.8 Pitch Array Interposer



0.076mm Preload Per Side

0.150mm Usable Travel Per Side

0.300mm Total Usable Travel

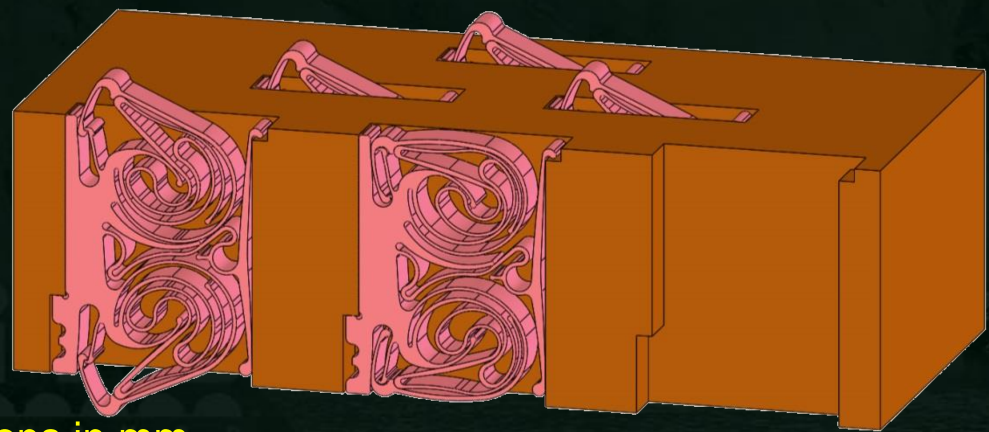
0.150mm Thickness

0.065mm Contact DUT Scrub/Side

1.0mm Fully compressed Height

Total Travel is ~31% of Height

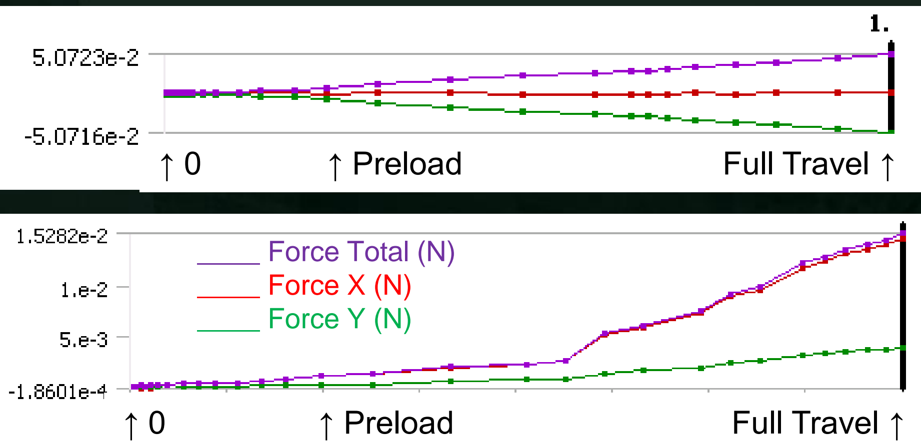
Force target per side ~8gf



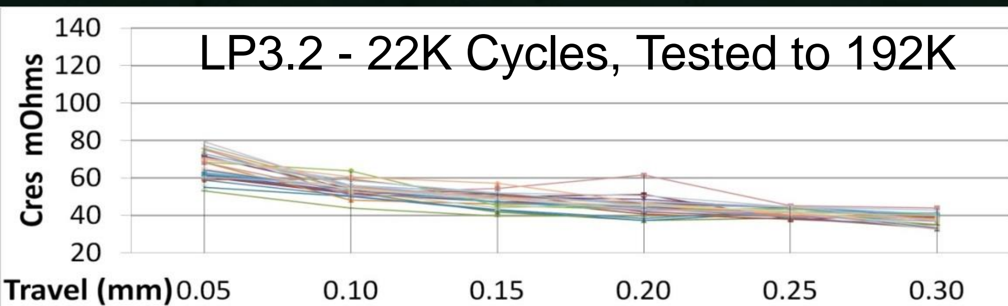
Targeted applications:
MLC, MLO to PCB
PCB-PCB
Test Sockets
OEM Sockets

Dimensions in mm

0.8mm Pitch Interposer Array

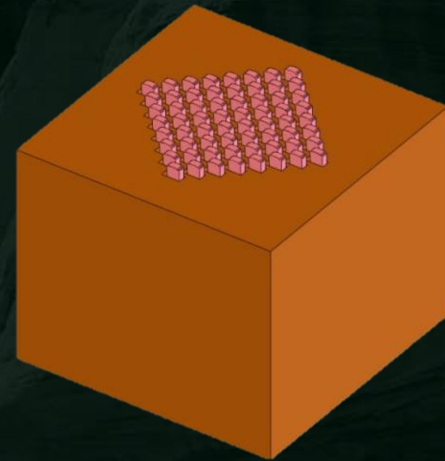


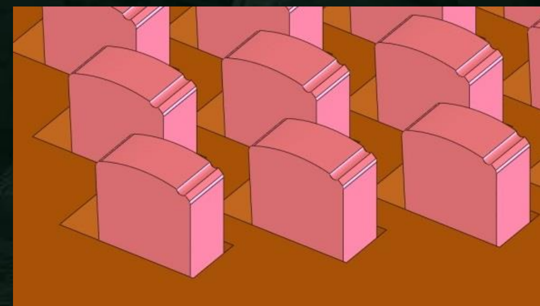
Design Goals
Low Force √
Short/Direct Signal Path √
Scrub/Wipe at Contact Surfaces √
Low & Consistence CRES √ *
Low Cost √ *
Well Suited for HVM Automation



WLCSP-CSP Interconnects (0.4 mm Shown)

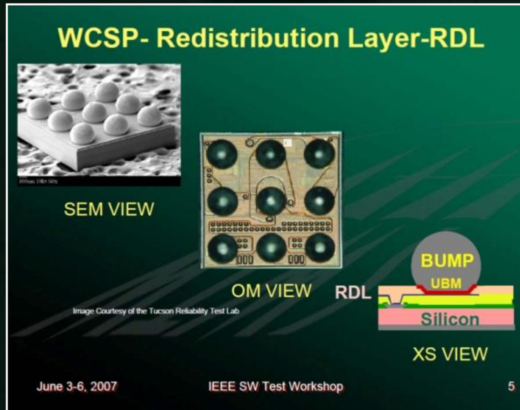
Design Goals
Low Force
Direct Signal Path
Scrub/Wipe at DUT Contact Surface
Low & Consistent CRES
Low Cost
HVM Automation
Array Pitches
- 0.8mm
- 0.4mm
- 0.3mm
- 0.2mm

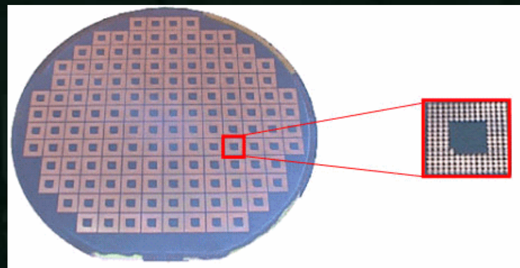




WLCSP Spring Pin Alternative

- 0.3 mm pitch array
- 4.2 mm compressed height
- 0.2 mm travel DUT side
- ~9 gf DUT side
- 0.15 mm travel PCB side





As Manufactured

Preloaded

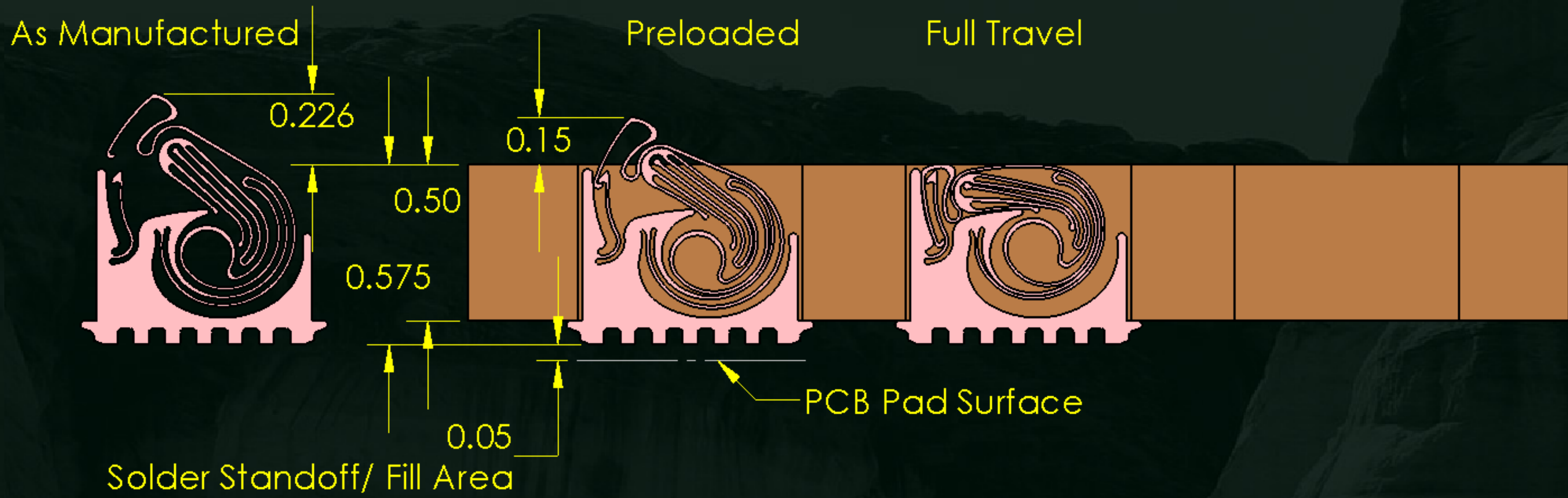
Full Travel

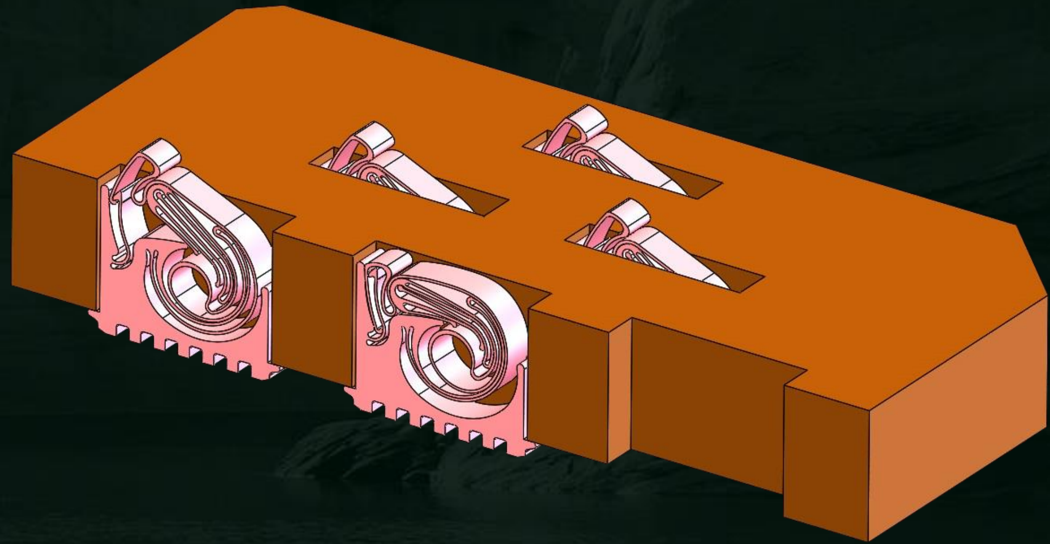
0.30 0.20

4.25

0.15

OEM Socket/Interposer SMT version (Socketed ASIC)

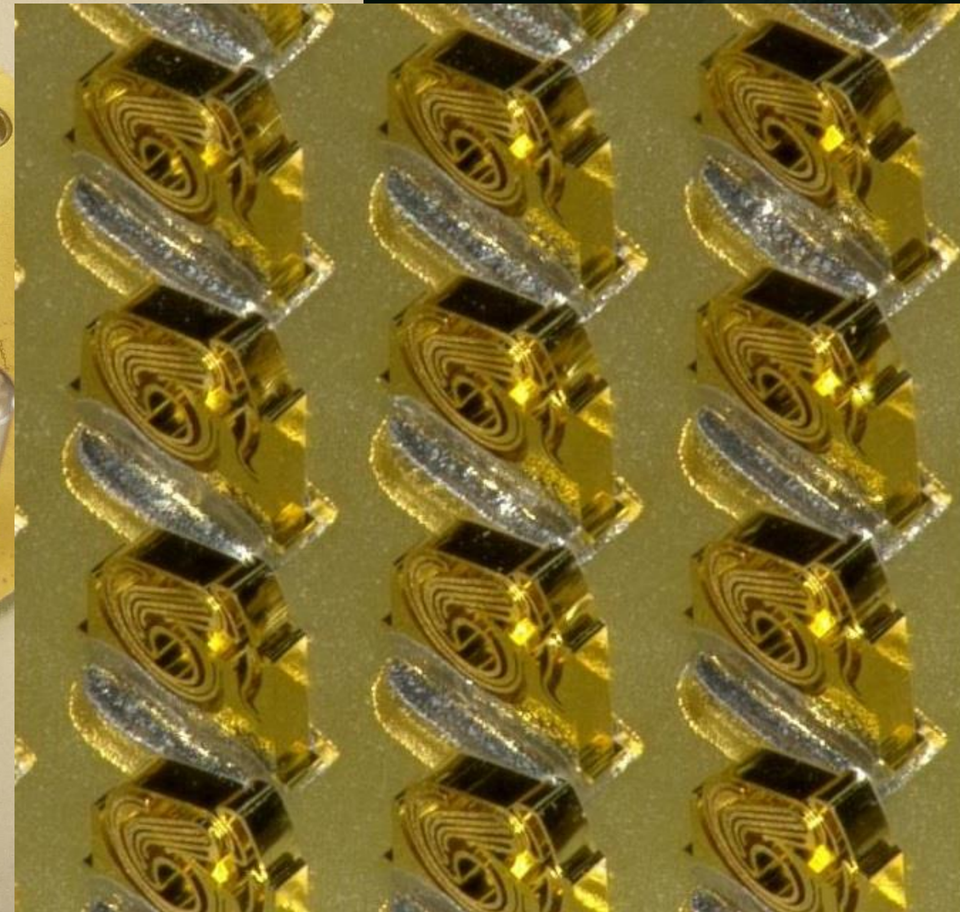




SMT Validation

50mm x 50mm PCB

8x8 pin array @ 0.7424mm pitch
(Pb free solder)



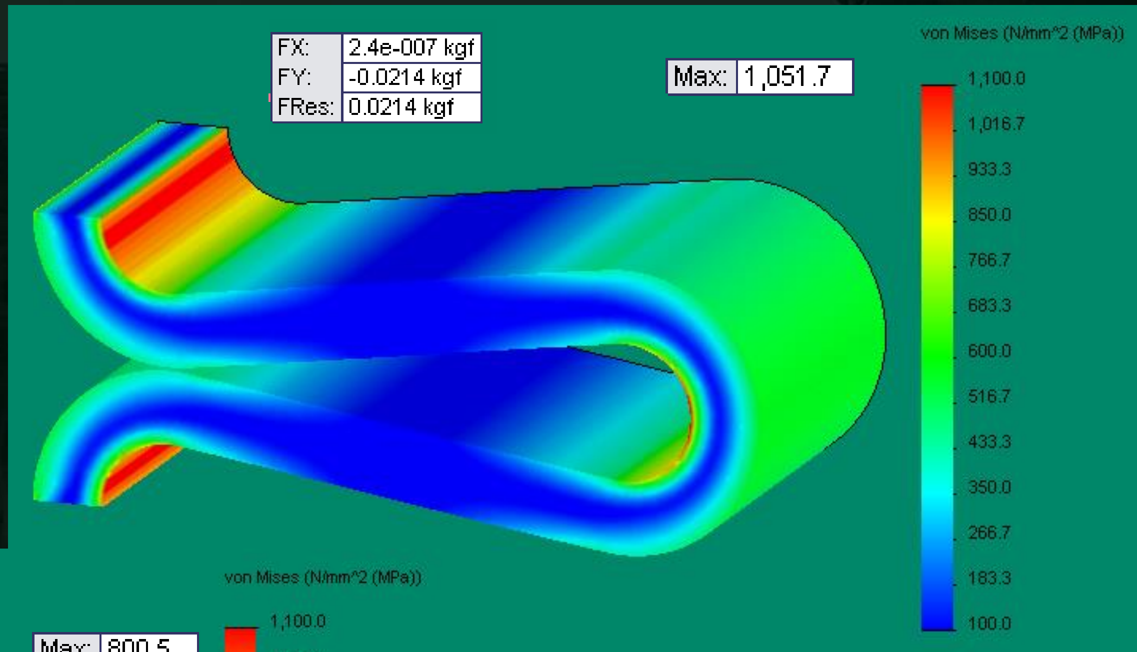
Design Advantages

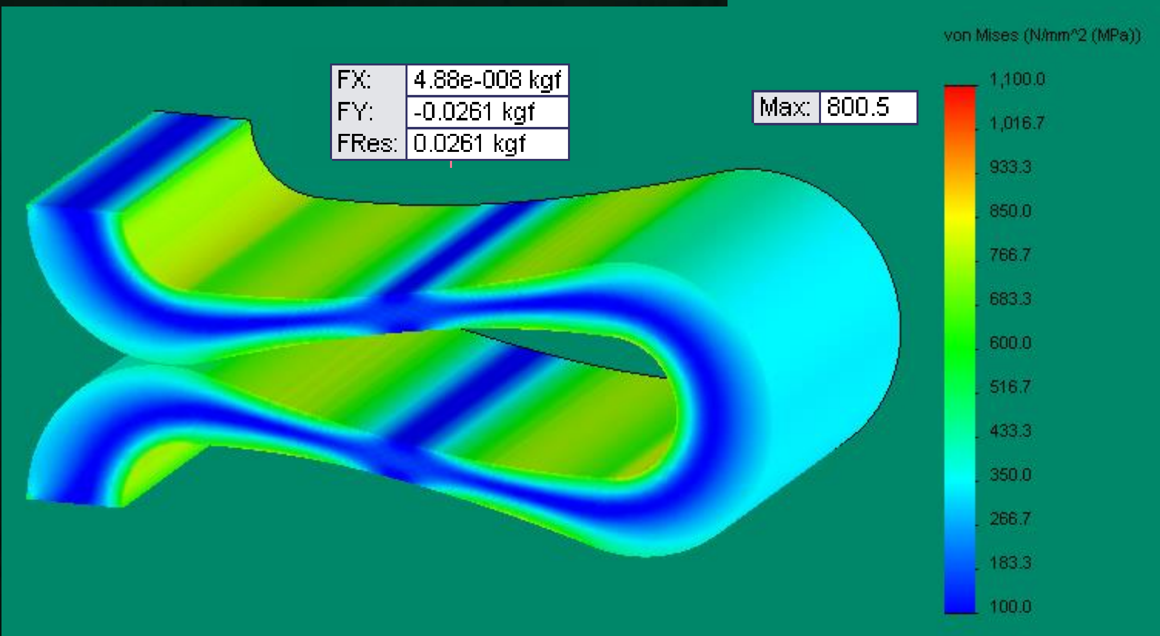
Allows for very efficient distribution and increased storage of strain energy

This example shows

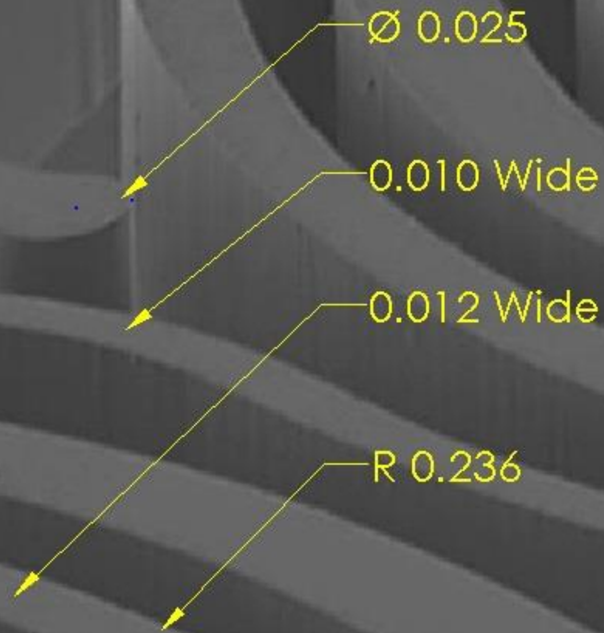
~23% less peak stress with
~22% more force

The only change is the tapering





Design Advantages

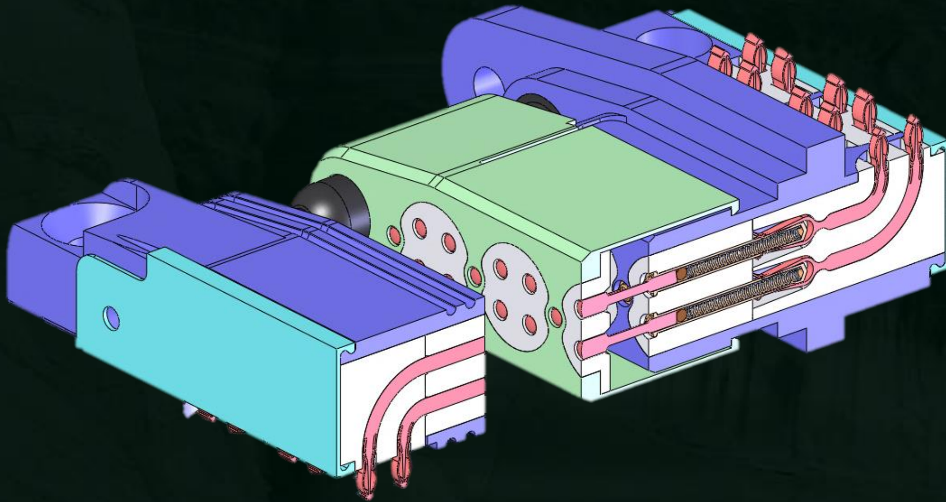


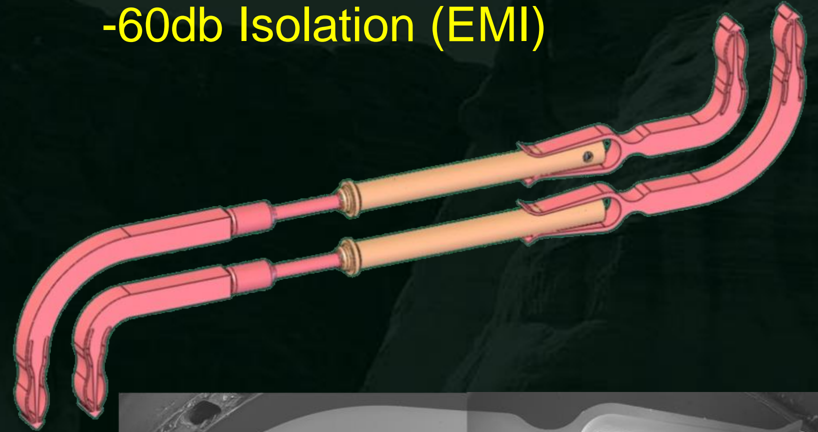
Design Advantages

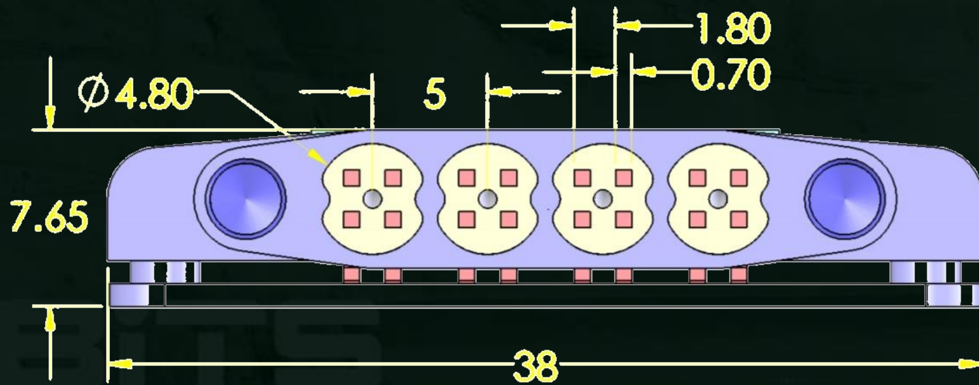
Prototype Flexibility

An effective Prototype Process

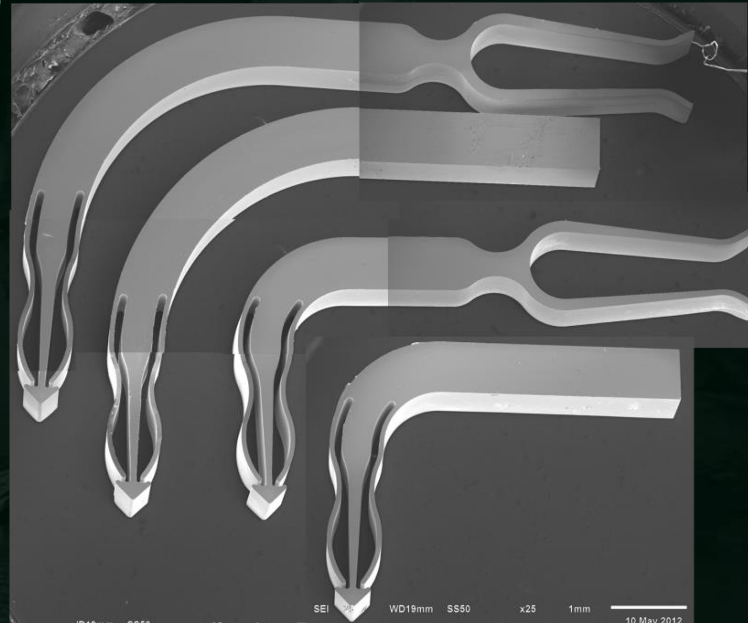
HDMI & USB 3.0 Signals, Power
-60db Isolation (EMI)







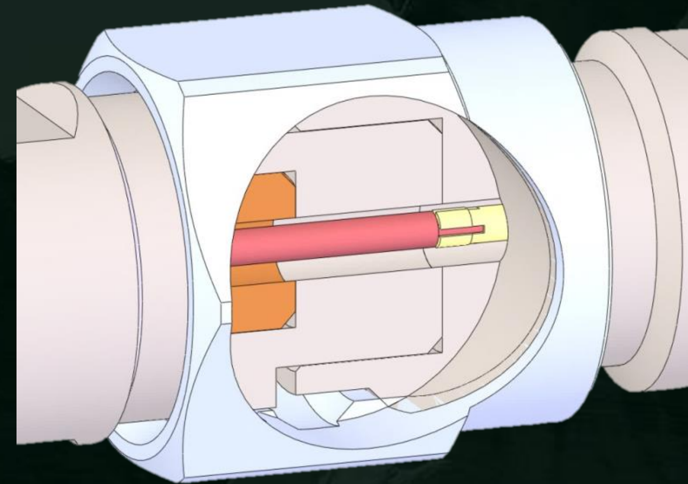
Dimensions in mm

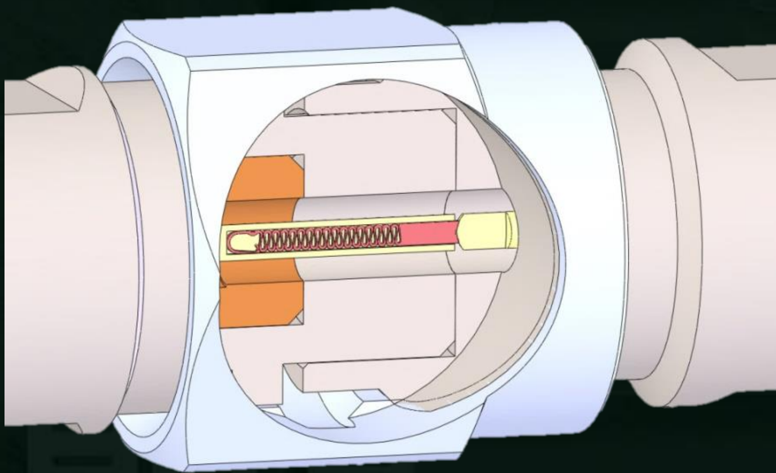


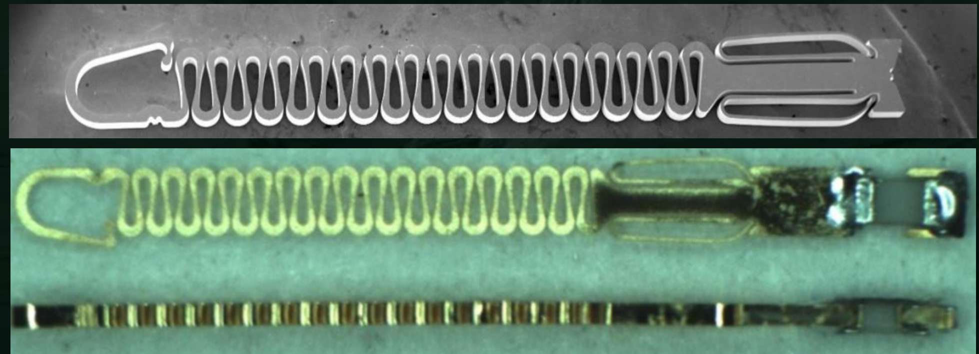
What if…, Could we…

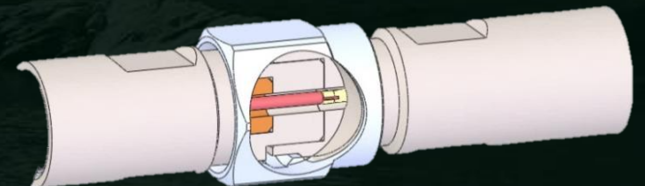
RPC-1.60 80Ghz Connector
Typical Pin & Socket Signal interconnect

Can we:
Improve the mating cycles -Yes
Improve the robustness -Yes
Improve the cost -Yes
Maintain the Signal Integrity - Close but No



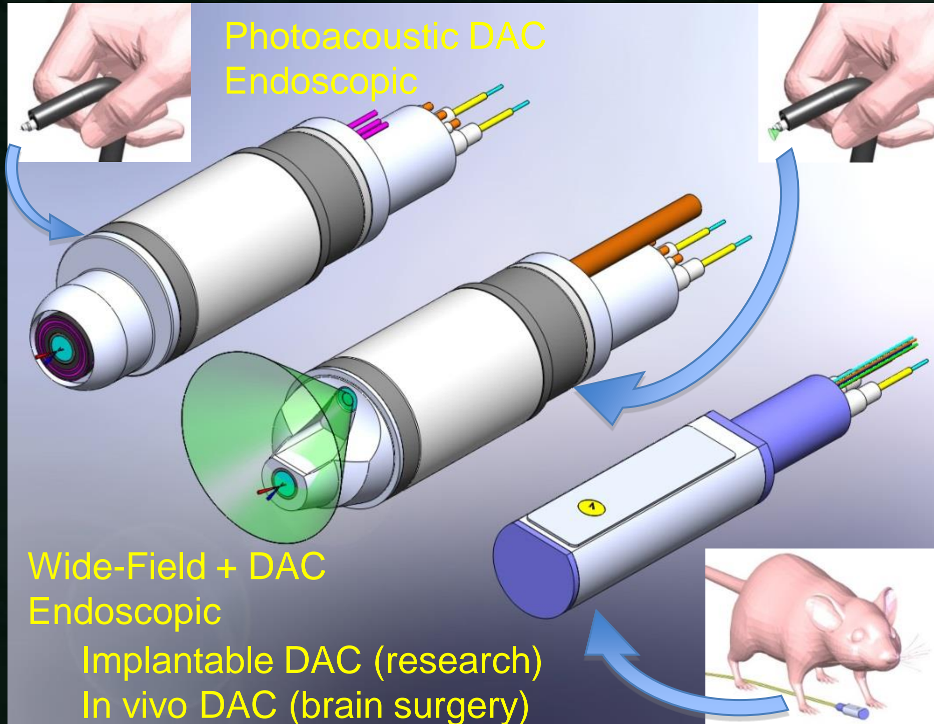


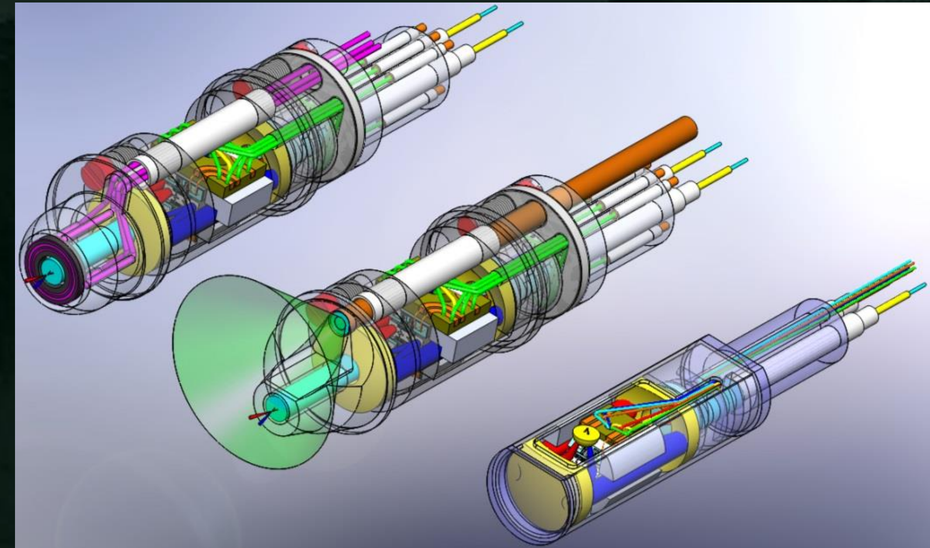


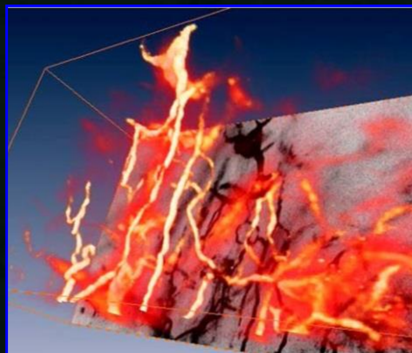


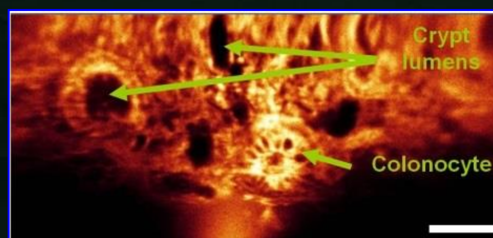
NTR-Clinical and Implantable Dual Axis Confocal (DAC) microscopes

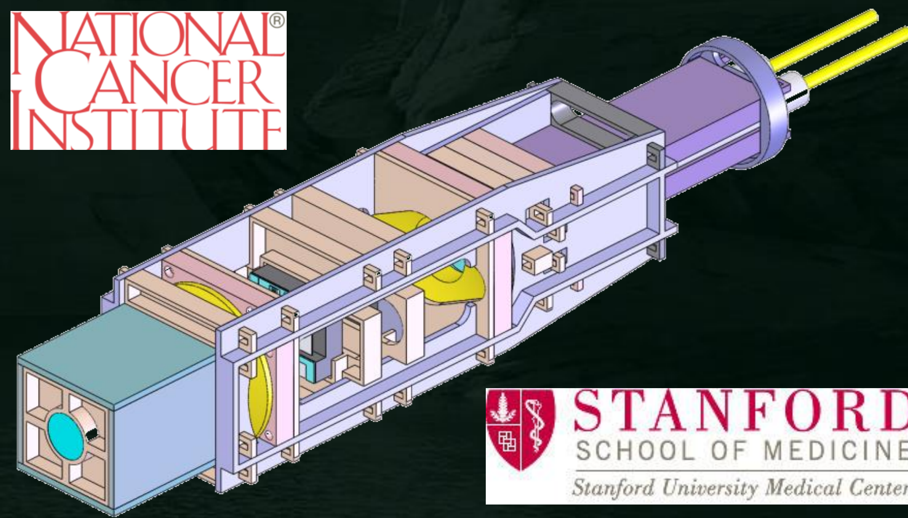
Endoscopic – In Vivo – Research Implantable











In Conclusion

LIGA is an advanced Microfabrication technology

LIGA is a technology well suited for enabling next generation interconnects designs

LIGA Microfabrication is only limited by one's imagination (and of course knowledge of the technology)

References

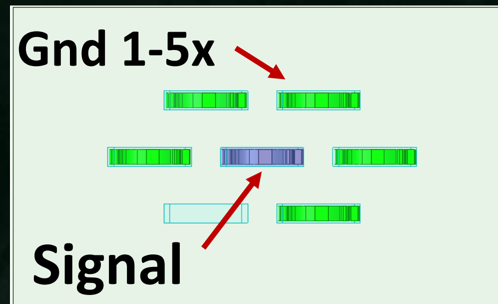
“LIGA and its Application to Electrical Interconnects”
IEEE SW Test Workshop 2012

“Iterative design approach requiring Multi-Physics analysis”
Ansys Santa Clara Conversance Conference 2013

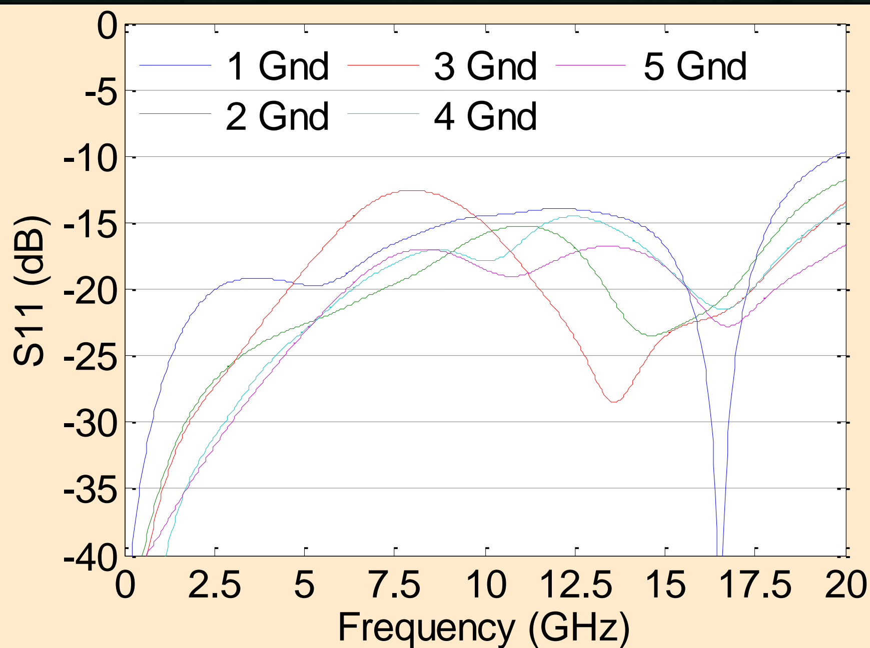
“Neat as a Pin”
Rosenberger leverages mechanical and electrical simulation to provide a superior alternative to traditional spring pins for semiconductor testing.
Ansys Advantage Magazine (June 2014 issue)

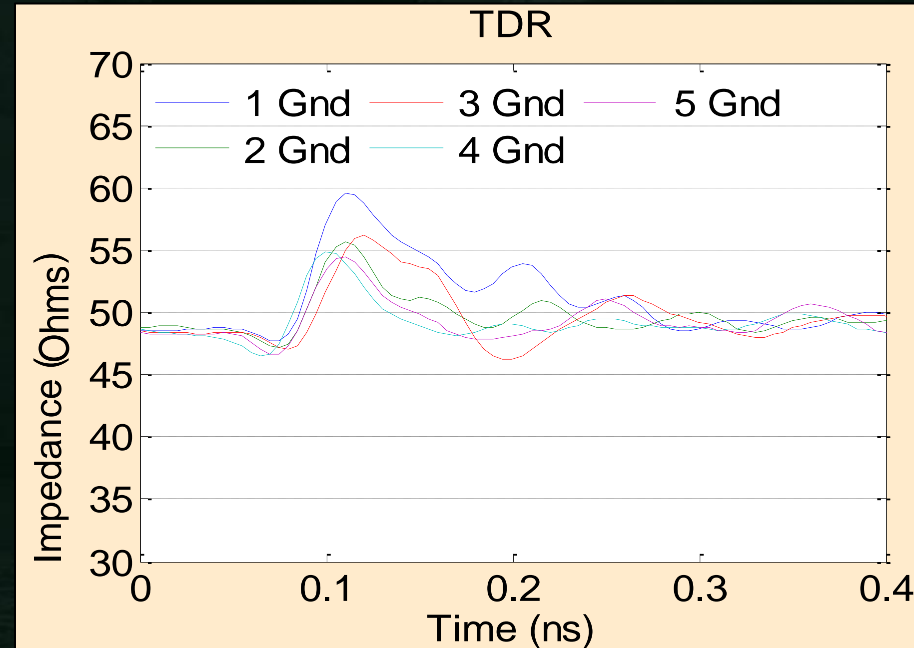
0.8 Pitch Measurements & Analysis

Pin configuration (Top view)

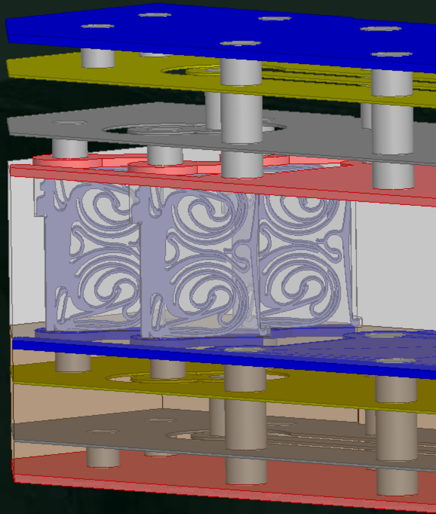


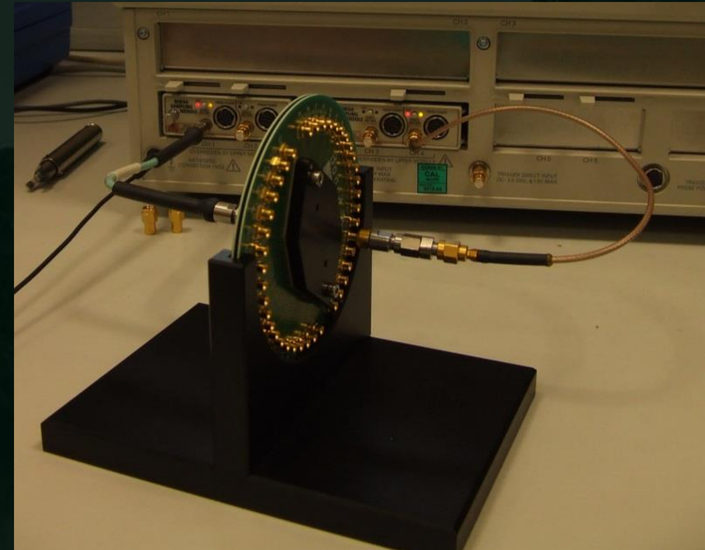
Config. (no. of returns)	Test fixture only 20-80 Risetime (ps)	Test fixture + MCI 20-80 Risetime (ps)	Equivalent BW (GHz)
1 GND	35.5	57.7	7.7
2 GND	35.1	56.3	8.0
3 GND	36.3	61.2	7.1
4 GND	36.8	52.6	9.3
5 GND	35.8	52.6	9.1

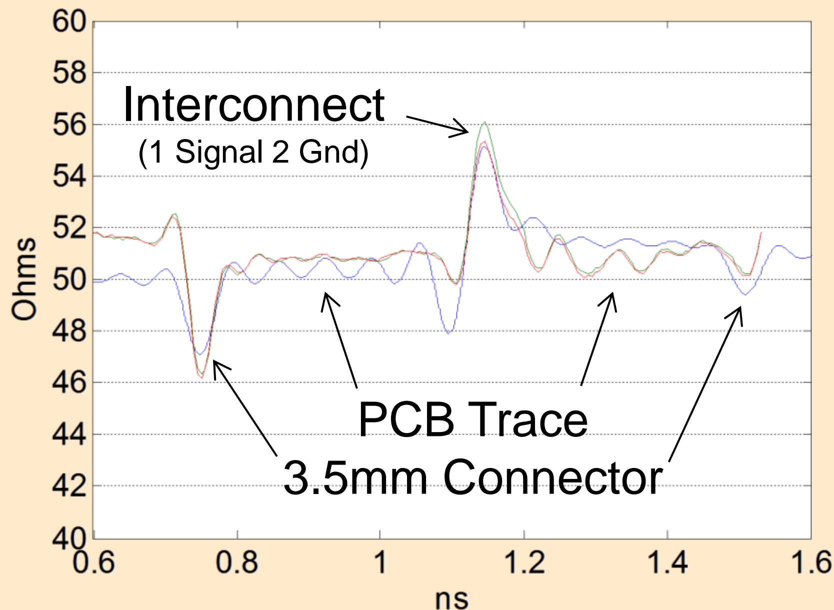




Simulation vs. Measurement







HFSS

Insufficient Compression (Measured)

Designed Compression (Measured)

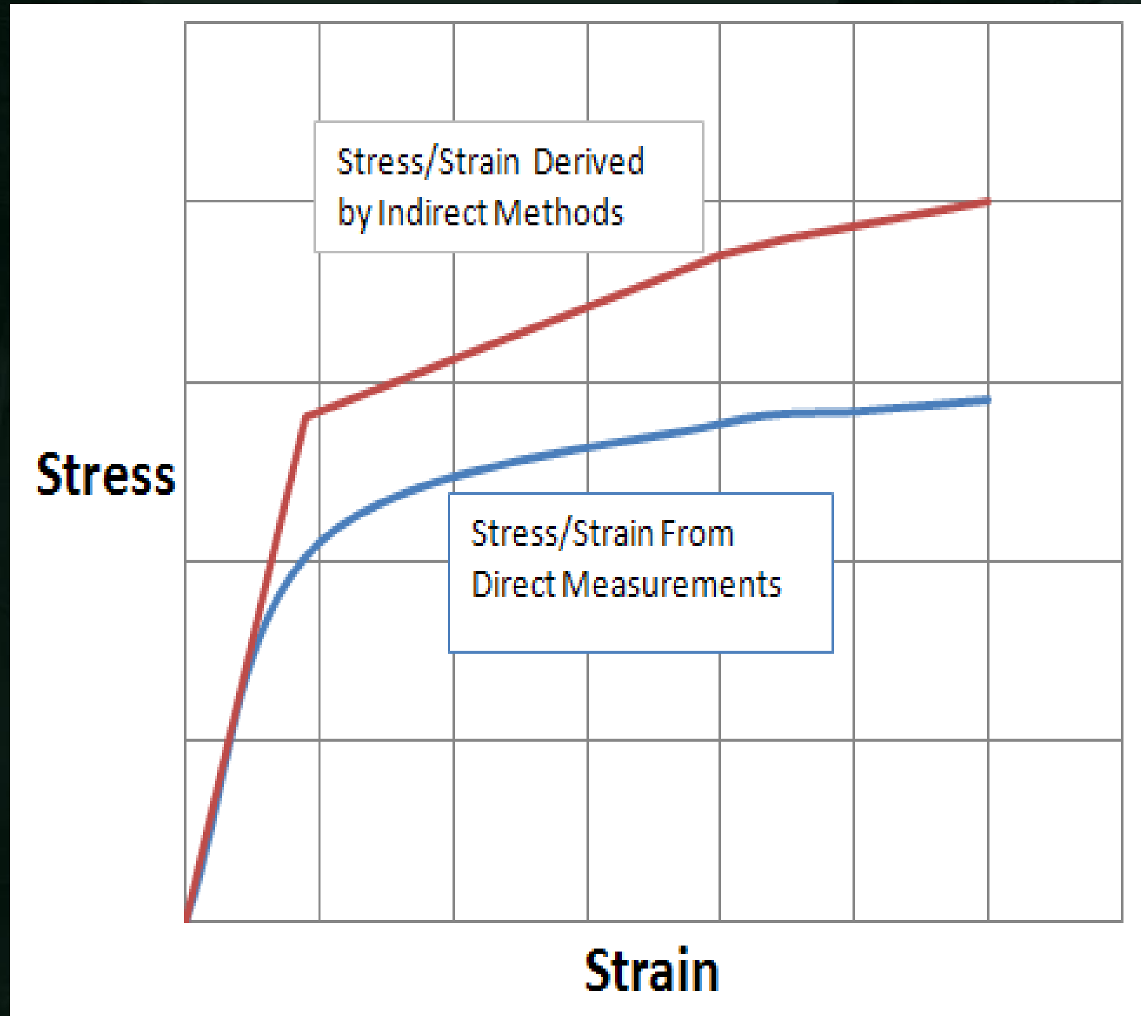
Material Properties Expectations Vs. Reality

Common industry (LIGA) practice is for mechanical properties to be indirectly derived from failure data.

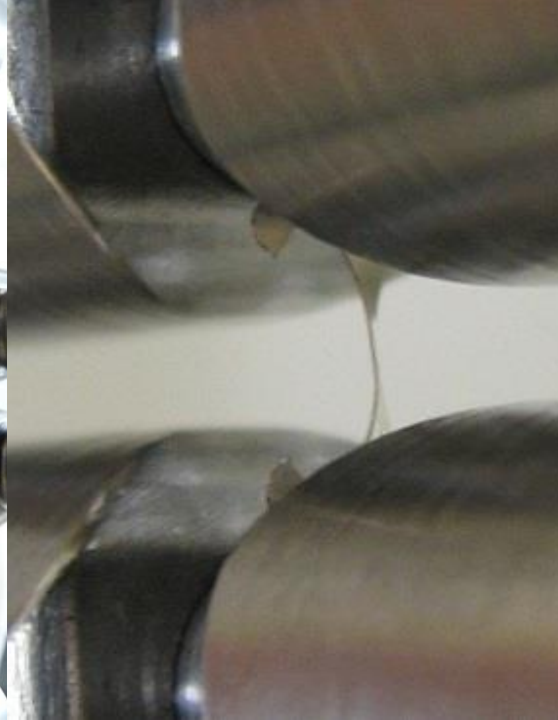
Current mechanical properties based on actual tests of micro samples.

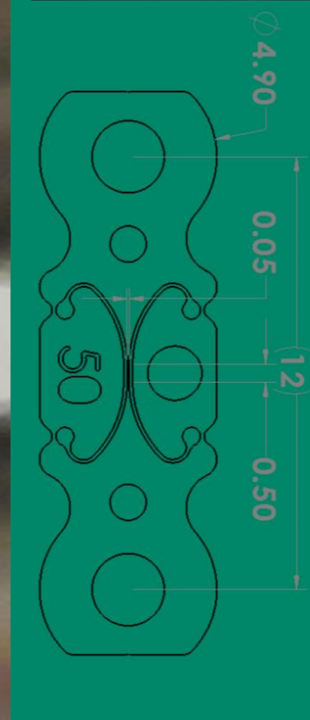
Precise Yield stress is difficult to define.

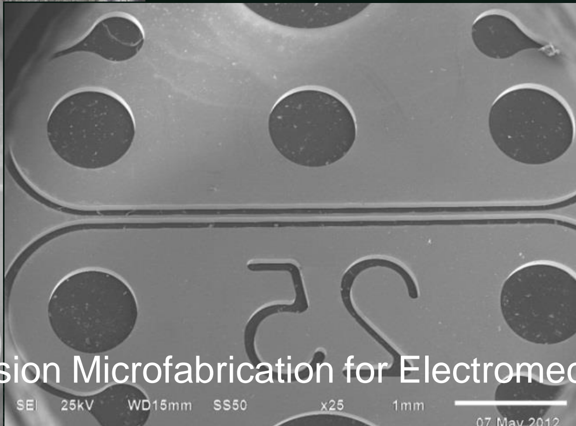
There is no substitute for direct measurements…

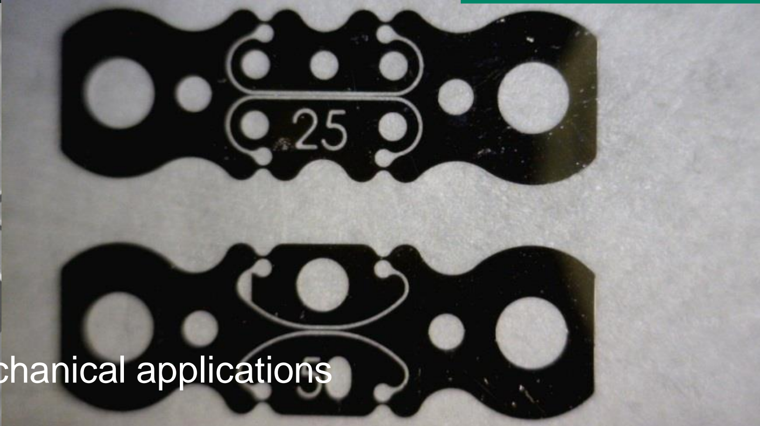


Material Properties
The solution

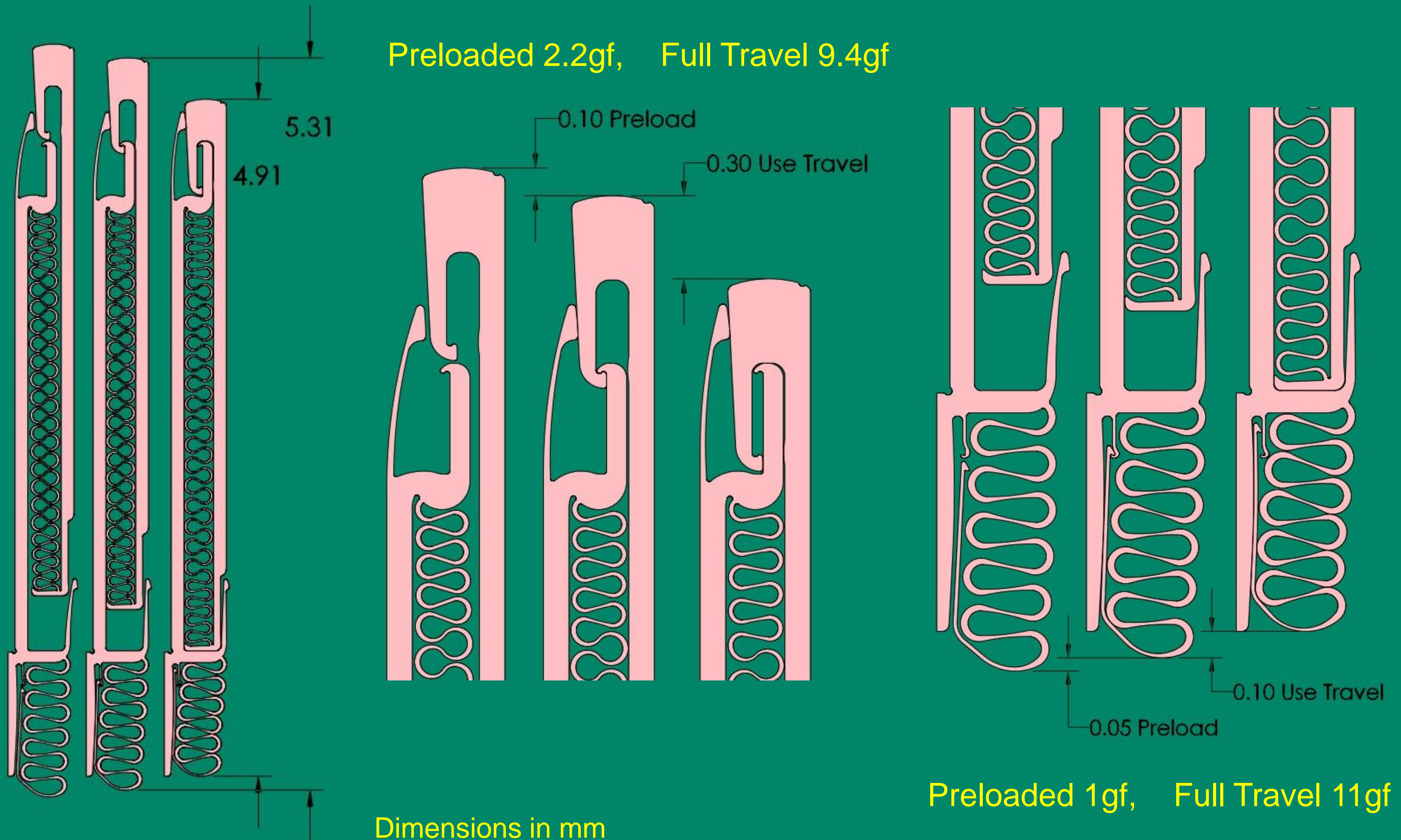








WLCSP-CSP Interconnects (0.4 mm Shown)



WLCSP-CSP Interconnects (0.4 mm Shown)